



**SPECIFICATION
FOR
LCD Module
PV04005TD25E-CO**

| | |
|------------------|-----------------|
| MODULE: | PV04005TD25E-CO |
| CUSTOMER: | |

| | INITIAL | DATE |
|--------------------|----------------|-------------|
| PREPARED BY | | 2019-10-25 |
| CHECKED BY | | 2019-10-25 |
| APPROVED BY | | 2019-10-25 |

| CUSTOMER | INITIAL | DATE |
|--------------------|----------------|-------------|
| APPROVED BY | | |



REVISION STATUS

| Version | Revise Date | Page | Content | Modified by |
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| V1.0 | 2019-10-25 | - | First Issued. | YANG |
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TABLE OF CONTENTS

- 1.General Description
2. Mechanical Characteristics
3. Pin Description
4. Electrical Characteristics
5. Optical Characteristics
6. Quality Specifications
7. Reliability
8. Handling Precaution
9. Packagingfigure



1. General Description

* DESCRIPTION

PV04005TD25E-CO is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.97" TFT-LCD contains 480 x 800 pixels, and can display up to 16.7M colors.

* Features

- Low Input Voltage: VCC: 2.5~3.3V;IOVCC: 1.65~3.3V
- Display Colors of TFT LCD: 16.7M colors
- Interface: MIPI-2 Lanes
- Internal Power Supply Circuit.

| General Information Items | Specification | Unit | Note |
|---------------------------|------------------------|---------|------|
| | Main Panel | | |
| Display area(AA) | 51.84(H) *86.4 (V) | mm | - |
| Driver element | a-Si TFT active matrix | - | - |
| Display colors | 16.7M | colors | - |
| Number of pixels | 480(RGB) *800 | dots | - |
| Pixel arrangement | RGB vertical stripe | - | - |
| Pixel pitch | 0.108 (H) *0.108(V) | mm | - |
| Viewing angle | All | o'clock | - |
| Drive IC | ST7701S | - | - |
| Display mode | Normally black | - | - |
| Operating temperature | -20~+60 | °C | - |
| Storage temperature | -30~+70 | °C | - |

Mechanical Information

| Item | | Min. | Typ. | Max. | Unit | Note |
|-------------|---------------|------|--------|------|------|-------|
| Module size | Horizontal(H) | - | 62.50 | - | mm | ±0.05 |
| | Vertical(V) | - | 111.04 | - | mm | ±0.05 |
| | Depth(D) | - | 3.47 | - | mm | ±0.15 |
| Weight | | - | TBD | - | g | - |



3.Pin Description

3.1 LCM

| Pin NO. | Symbol | Level | Function |
|---------|--------|-------|--|
| 1 | LEDA | H | Backlight+ |
| 2 | LEDK | L | Backlight- |
| 3 | GND | L | Ground |
| 4 | NC | | NC |
| 5 | NC | | NC |
| 6 | GND | L | Ground |
| 7 | TDPO | H/L | HSSI_D0+ are differential data signal line. |
| 8 | TDN 0 | H/L | HSSI_D0- are differential data signal line. |
| 9 | GND | L | Ground |
| 10 | TCP | H/L | HSSI_CLK+ are differential data signal line. |
| 11 | TCN | H/L | HSSI_CLK- are differential data signal line. |
| 12 | GND | L | Ground |
| 13 | TDP 1 | H/L | HSSI_D1+ are differential data signal line. |
| 14 | TDN 1 | H/L | HSSI_D1- are differential data signal line. |
| 15 | GND | L | Ground |
| 16 | NC | | NC |
| 17 | NC | | NC |
| 18 | GND | L | Ground |
| 19 | RST | H/L | Hardware reset pin |
| 20 | TE | H/L | Tearing effect output |
| 21 | ID | H | P Connctet 10K resistance to GND) |
| 22 | VDD | H | Power supply(2.5-3.3V) |
| 23 | GND | L | Ground |
| 24 | IOVCC | H | Power supply(1.65-3.3V) |
| 25 | GND | L | Ground |



3.2 CTP

| Pin NO. | Symbol | Function |
|---------|---------|--|
| 1 | NC | Not Connect |
| 2 | GND | Ground |
| 3 | GND | Ground |
| 4 | SCL | Serial clock input |
| 5 | SDA | Serial data input pin |
| 6 | VDD2.8V | Power supply to the internal logic power regulator |
| 7 | INT | Interrupt pin |
| 8 | RESET | Reset pin |
| 9 | NC | Not Connect |
| 10 | GND | Ground |
| 11 | GND | Ground |
| 12 | NC | Not Connect |
| 13 | NC | Not Connect |



4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Values | | Unit | Remark |
|-----------------------------------|--------|--------|------|------|--------|
| | | Min | Max. | | |
| Supply Voltage for Logic circuit | VDDIO | 1.65 | 3.3 | V | |
| Supply Voltage for analog circuit | Vcc | 2.5 | 3.3 | V | |

4.2 DC ELECTRICAL CHARACTERISTICS

4.2.1 OPERATING CONDITIONS

Typical Operating Conditions (Ta=25°C)

| Item | Symbol | Values | | | Unit | Remark |
|---------------------------------|-----------------|--------|-----|------|------|----------|
| | | Min | Typ | Max. | | |
| Power Supply | Vcc | 2.5 | 2.8 | 3.3 | V | |
| Power Supply | VDDIO | 1.65 | 1.8 | 3.3 | V | |
| Normal mode Current consumption | Icc | - | 80 | - | mA | VCC=2.8V |
| TFT Gate ON Voltage | V _{GH} | 10 | - | 20 | V | |
| TFT Gate OFF Voltage | V _{GL} | -15 | - | -7.5 | V | |

4.2.2 BACKLIGHT UNIT (GND=0V)

| Item | Symbol | Values | | | Unit | Remark |
|------------------------|----------------|--------|-----|------|-------------------|----------------------|
| | | Min | Typ | Max. | | |
| Forward supply Voltage | V _f | 11.6 | | 13.6 | V | |
| Forward supply Current | I _f | - | 40 | - | mA | |
| LCM Luminance | L _v | 350 | 400 | - | cd/m ² | I _B =40mA |
| Uniformity | / | 80 | | | % | - |



4.3 MIPI Interface Characteristics

4.3.1

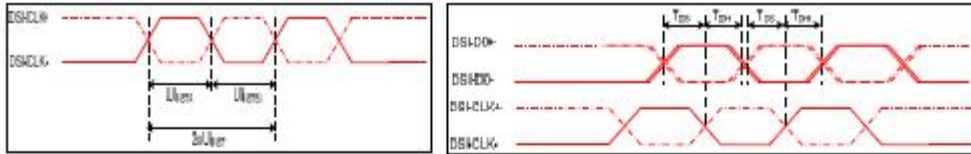


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDD1=1, VDD=2 & AGND=DGND=0V, Ta=25 °C

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|------------|--|--------------------------|------|------|------|--|
| DSI-CLK+/- | 2xUI _{INSTA} | Double UI instantaneous | 4 | 25 | ns | |
| DSI-CLK+/- | UI _{INSTA} UI _{INSTB} | UI instantaneous halves | 2 | 12.5 | ns | UI = UI _{INSTA} = UI _{INSTB} |
| DSI-Dn+/- | tDS | Data to clock setup time | 0.15 | - | UI | |
| DSI-Dn+/- | tDH | Data to clock hold time | 0.15 | - | UI | |

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

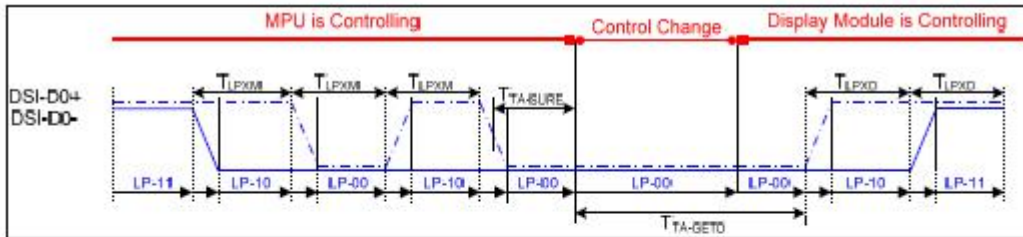


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

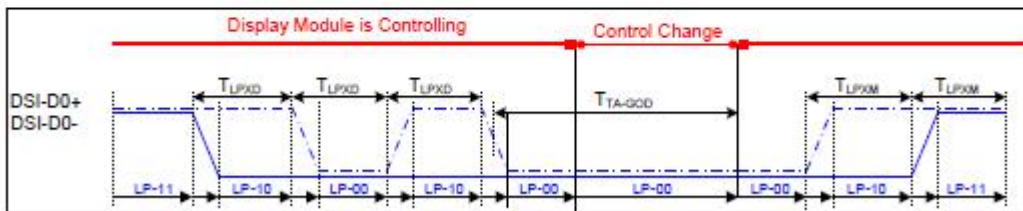


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing



DSI clock Timing

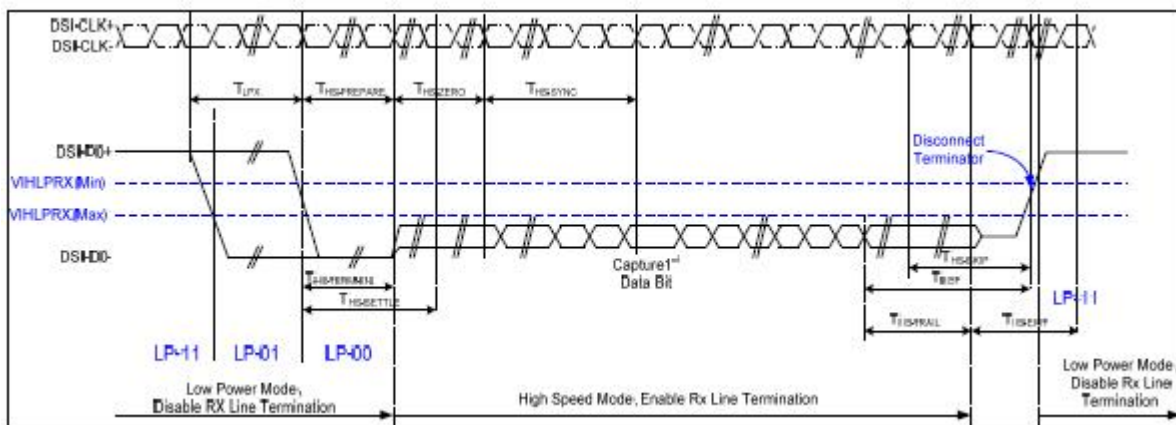
Characteristics

Rising and falling time on clock and data channel

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|-----------|-----------|--|---------------------|---------------------|------|-------------|
| DSI-D0+/- | TLPXM | Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module | 50 | 75 | ns | Input |
| DSI-D0+/- | TLPXD | Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module | 50 | 75 | ns | Output |
| DSI-D0+/- | TTA-SURED | Time-out before the MPU start driving | T_{LPXD} | $2 \times T_{LPXD}$ | ns | Output |
| DSI-D0+/- | TTA-GETD | Time to drive LP-00 by display module | $5 \times T_{LPXD}$ | | ns | Input |
| DSI-D0+/- | TTA-GOD | Time to drive LP-00 after turnaround request-MPU | $4 \times T_{LPXD}$ | | ns | Output |

DSI High Speed Mode characteristics

4.32



BTA from HOST to Display module Timing

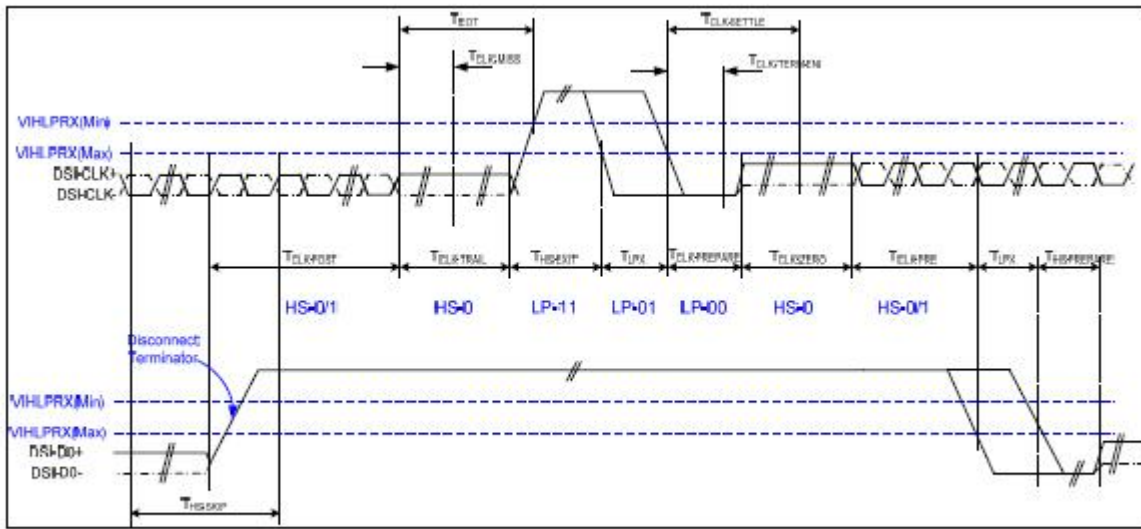


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

BTA from Display module Timing to HOST



| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|--------------------------|--|--------------|--------------------|------|-------------|
| Low Power Mode to High Speed Mode Timing | | | | | | |
| DSI-Dn+/- | TLPX | Length of any low power state period | 50 | - | ns | Input |
| DSI-Dn+/- | THS-PREPARE | Time to drive LP-00 to prepare for HS transmission | 40+4 UI | 85+6 UI | ns | Input |
| DSI-Dn+/- | THS-TERM-EN | Time to enable data receiver line termination measured from when Dn crosses VILMAX | - | 35+4 UI | ns | Input |
| DSI-Dn+/- | THS-PREPARE + THS-ZERO | THS-PREPARE + time to drive HS-0 before the sync sequence | 140+ 10UI | - | ns | Input |
| High Speed Mode to Low Power Mode Timing | | | | | | |
| DSI-Dn+/- | THS-SKIP | Time-out at display module to ignore transition period of EoT | 40 | 55+4 UI | ns | Input |
| DSI-Dn+/- | THS-EXIT | Time to drive LP-11 after HS burst | 100 | - | ns | Input |
| DSI-Dn+/- | THS-TRAIL | Time to drive flipped differential state after last payload data bit of a HS transmission burst | 60+4 UI | - | ns | Input |
| High Speed Mode to/from Low Power Mode Timing | | | | | | |
| DSI-CLK+/- | TCLK-POS | Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode | 60+5 2UI | - | ns | Input |
| DSI-CLK+/- | TCLK-TRAIL | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns | Input |
| DSI-CLK+/- | THS-EXIT | Time to drive LP-11 after HS burst | 100 | - | ns | Input |
| DSI-CLK+/- | TCLK-PREPARE | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns | Input |
| DSI-CLK+/- | TCLK-TERM-EN | Time-out at clock lan display module to enable HS transmission | -- | 38 | ns | Input |
| DSI-CLK+/- | TCLK-PREPARE + TCLK-ZERO | Minimum lead HS-0 drive period before starting clock | 300 | - | ns | Input |
| DSI-CLK+/- | TCLK-PRE | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8UI | - | ns | Input |
| DSI-CLK+/- | TEOT | Time form start of TCLK-TRAIL period to start of LP-11 state | - | 105n s+12 UI | ns | Input |



7.5.5 Reset Timing:

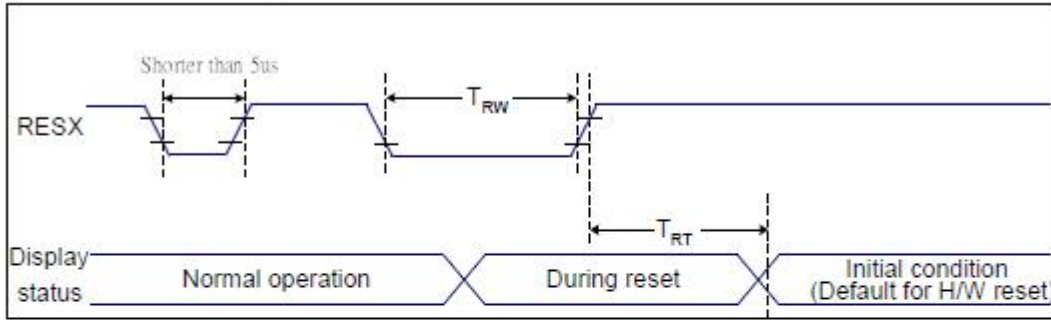


Figure 9 Reset Timing

VDD1=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|--------------|--------|----------------------|--------------------|---------------|------|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| - | | | 120 (Note 1, 6, 7) | ms | |

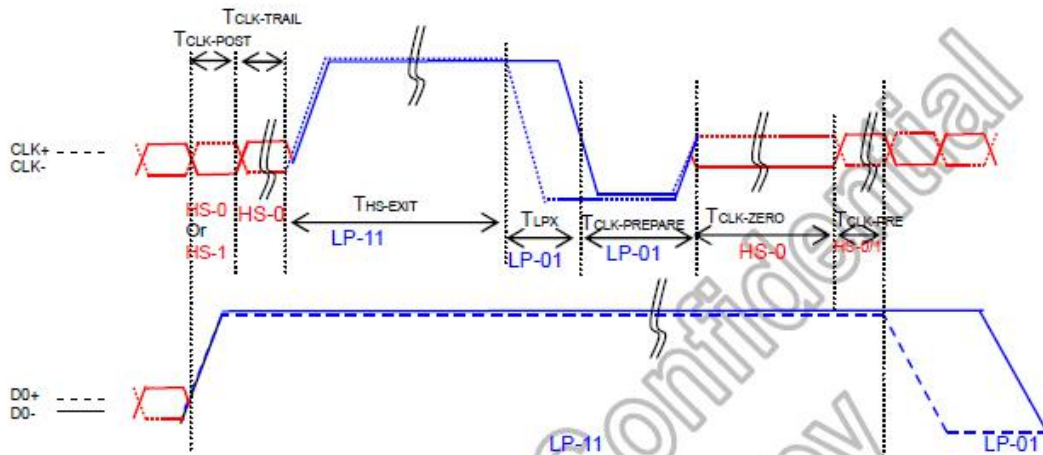
Table 9 Reset Timing

Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (TRT) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

| RESX Pulse | Action |
|---------------------|----------------|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

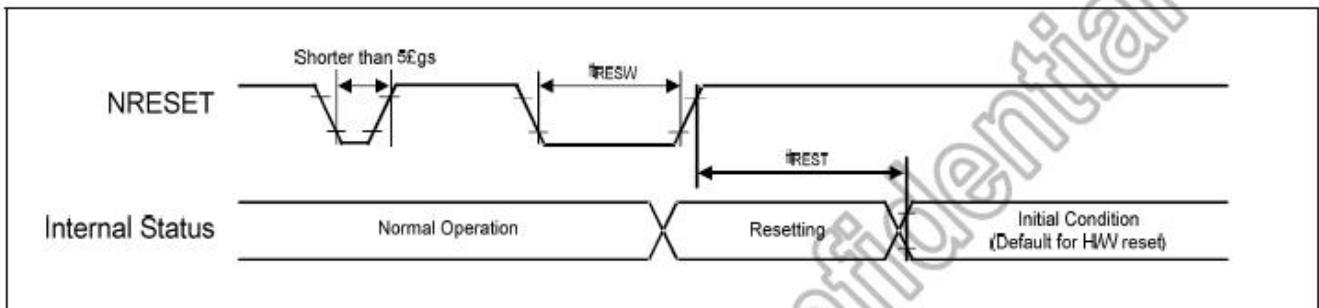
- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode.) and then return to Default condition for Hardware Reset.
- Spike Rejection also applies during a valid reset pulse as shown below:



| Signal | Item | Symbol | Spec. | | | Unit |
|-------------------|--|--------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| DSI_CP/ DSI_CN | Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | TCLK-POST | 60+52xUI | - | - | ns |
| | Time to drive HS differential state after last payload clock bit of a HS transmission burst | TCLK-TRAIL | 60 | - | - | ns |
| | Time to drive LP-11 after HS burst | THS-EXIT | 100 | - | - | ns |
| | Time to drive LP-00 to prepare for HS transmission | TCLK-PREPARE | 38 | - | 95 | ns |
| | Time-out at Clock Lane Display Module to enable HS Termination | TCLK-TERM-EN | - | - | 38 | ns |
| | Minimum lead HS-0 drive period before starting Clock | TCLK-PREPARE + TCLK-ZERO | 300 | - | - | ns |
| | Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode | TCLK-PRE | 8xUI | | | |

Clock Lanes High Speed Mode to/from Low Power Mode Timings

4.3.2. Reset input timing



Reset input timing



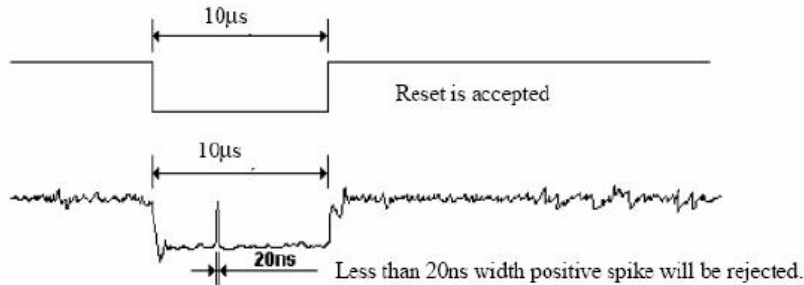
| Symbol | Parameter | Related Pins | Spec. | | | Note | Unit |
|--------|--------------------------------------|--------------|-------|------|------|---------------------------------------|------|
| | | | Min. | Typ. | Max. | | |
| tRESW | Reset low pulse width ⁽¹⁾ | NRESET | 10 | - | - | - | μs |
| tREST | Reset complete time ⁽²⁾ | - | 5 | - | - | When reset applied during SLPIN mode | ms |
| | | - | 120 | - | - | When reset applied during SLPOUT mode | ms |

Reset input timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

| NRESET Pulse | Action |
|------------------------|----------------|
| Shorter than 5 μs | Reset Rejected |
| Longer than 10 μs | Reset |
| Between 5 μs and 10 μs | Reset Start |

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is HW reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



- (5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.



5. OPTICAL CHARACTERISTICS

(LCD optical specification)

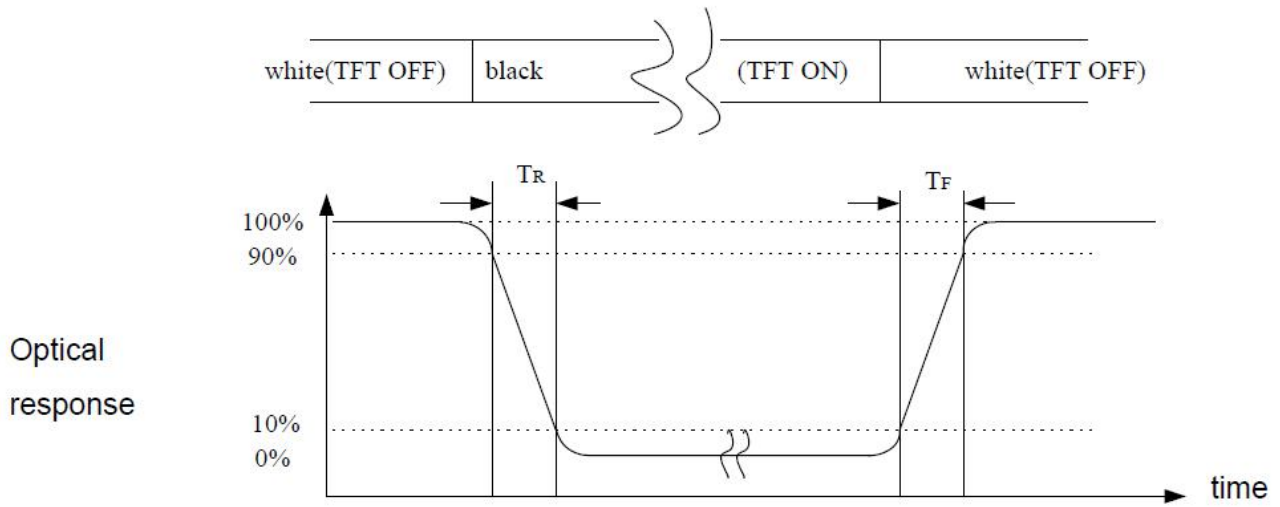
| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|-----------------------------------|---------|----------------|-----------------------------|-------|-------|-------|---|---|
| Transmittance (with Polarizer) | | T (%) | θ=0 Normal viewing angle | — | 4.14 | — | % | Measuring with Polarizer , Reference Only |
| Transmittance (without Polarizer) | | T (%) | | — | 13.13 | — | % | |
| Contrast | | CR | | 720 | 900 | — | — | (1)(2) |
| Response time | Rising | T _R | | — | 16 | 21 | msec | (1)(3) |
| | Falling | T _F | | — | 19 | 24 | | |
| Color gamut | | (%) | | — | 70 | — | % | C-light |
| Color chromaticity (CIE1931) | White | W _x | | -0.02 | 0.310 | +0.02 | — | (1)(4) CF glass |
| | | W _y | 0.336 | | | | | |
| | Red | R _x | 0.647 | | | | | |
| | | R _y | 0.317 | | | | | |
| | Green | G _x | 0.275 | | | | | |
| | | G _y | 0.582 | | | | | |
| | Blue | B _x | 0.140 | | | | | |
| | | B _y | 0.088 | | | | | |
| Viewing angle | Hor. | θ _L | CR>10 | — | 80 | — | (1)(4) Measuring with Polarizer , Reference Only | |
| | | θ _R | | — | 80 | — | | |
| | Ver. | θ _U | | — | 80 | — | | |
| | | θ _D | | — | 80 | — | | |
| Optima View Direction | | Free | | | | | (5) | |

Measuring Condition

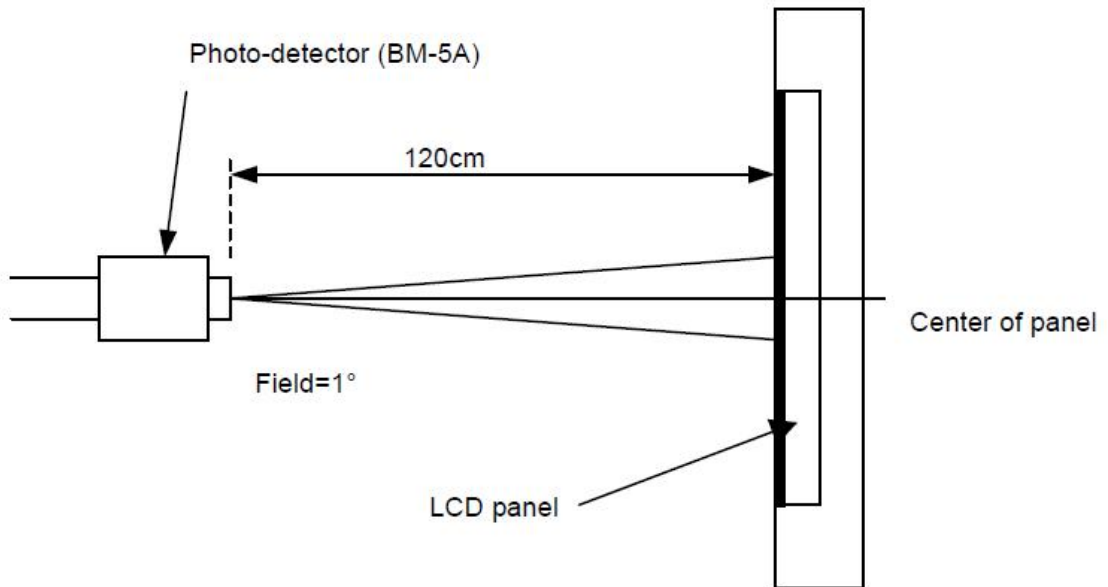
- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.



Note (3) Definition of Response Time : Sum of T_R and T_F

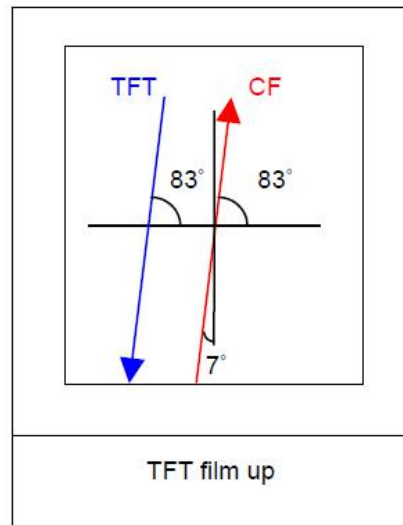


Note (4) Definition of optical measurement setup





Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



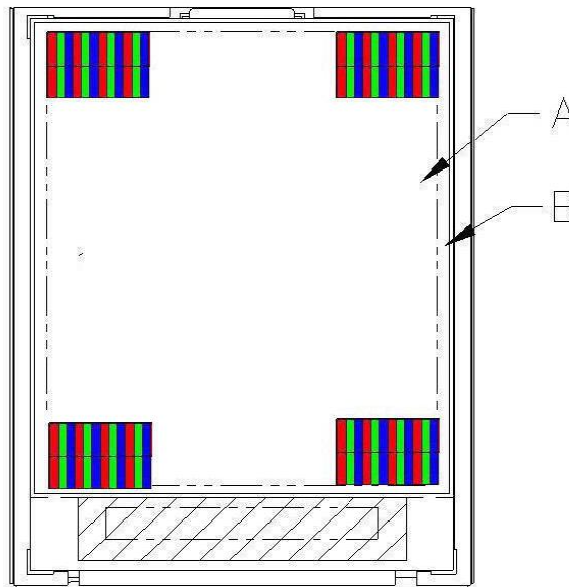


6. QUALITY SPECIFICATIONS

6.1 INSPECTION CONDITION

- (1) Inspect under 300~500Lux fluorescent light, leaving 30~35cm between panels and eyes, and between panels and lights.
- (2) Inspection condition is $23\pm 5^{\circ}\text{C}$, $50\pm 20\%RH$ maximum.

6.2 DEFINITION OF AREA





A Area : Viewing area.

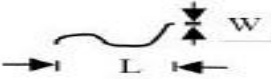
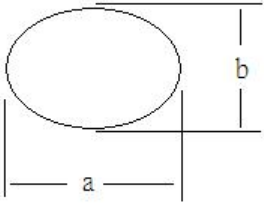
B Area : Out of viewing.(outside viewing area)



6.3 INSPECTION SPECIFICATION

| NO | Item | Acceptable specification | Judgment Criterion |
|----|----------------------|---|---|
| 1 | Electrical Testing | <p>1-1 sub pixel classification</p> <ul style="list-style-type: none"> ● Sub Pixel: Number of sub pixel doesn't exceed one dot. <div style="text-align: center;">  <p>Sub Pixel (Dot)</p> </div> <p>a > Dark dot ----one Allowed b > Bright dot ---- one Allowed</p> <ul style="list-style-type: none"> ● Pixel : Three dots link together doesn't exceed ones <div style="text-align: center;">  <p>Pixel</p> </div> <p>1-2 Leakage to light</p> <ul style="list-style-type: none"> ● Leakage to light be not allowed. <p>1-3 Picture to shake</p> <ul style="list-style-type: none"> ● Picture had shake, twinkle and noise etc. instable of defect that be not allowed. <p>1-4 Function</p> <ul style="list-style-type: none"> ● No display or No function. ● Source Line, Gate Line. ● Contrast Ratio ● Current consumption exceeds product specifications. ● Display malfunction. | <p>$N \leq 2$</p> <p>$N \leq 0$</p> <p>$N=0$</p> <p>$N=0$</p> <p>$N=0$</p> |
| 2 | Mechanical Dimension | <p>2-1 Mechanical Dimension exceeds product specifications. 2-2 Out of frame and boss of plastic changed shape that be not allowed.</p> | <p>$N=0$</p> |



| NO | Item | Acceptable specification | Judgment Criterion | | | | | | | | | | | | | | | | | | |
|--|---------------------|--|----------------------|-------------------|-------------------|------------------|-------------------------|---------------|-------------------------|---------------|--------------|-------------------------|---|---------------|----------------------|-----|----|------------|-------------|-----|--|
| 3 | Cosmetic Inspection | <p>3-1 Blemish: Line shapes of defect</p> <table border="1"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable number</th> <th>Mini. space</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.05$</td> <td>Ignore</td> <td rowspan="3">5 m m</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.05 < W \leq 0.08$</td> <td>4</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.08 < W \leq 0.15$</td> <td>3</td> </tr> <tr> <td>--</td> <td>$W > 0.15$</td> <td>Not allowed</td> <td>---</td> </tr> </tbody> </table> <p>L: length(mm) W: width(mm)</p>  | Length | Width | Acceptable number | Mini. space | --- | $W \leq 0.05$ | Ignore | 5 m m | $L \leq 3.0$ | $0.05 < W \leq 0.08$ | 4 | $L \leq 3.0$ | $0.08 < W \leq 0.15$ | 3 | -- | $W > 0.15$ | Not allowed | --- | |
| | | Length | Width | Acceptable number | Mini. space | | | | | | | | | | | | | | | | |
| | | --- | $W \leq 0.05$ | Ignore | 5 m m | | | | | | | | | | | | | | | | |
| | | $L \leq 3.0$ | $0.05 < W \leq 0.08$ | 4 | | | | | | | | | | | | | | | | | |
| | | $L \leq 3.0$ | $0.08 < W \leq 0.15$ | 3 | | | | | | | | | | | | | | | | | |
| | | -- | $W > 0.15$ | Not allowed | --- | | | | | | | | | | | | | | | | |
| | | <p>3-2 Blemish: dot shapes of defect.</p> <table border="1"> <thead> <tr> <th>Dimension</th> <th>Acceptable number</th> <th>Mini. Space</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td> <td>Ignore</td> <td>---</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td>3</td> <td rowspan="2">5 m m</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td>2</td> </tr> <tr> <td>$\Phi > 0.30$</td> <td>0</td> <td>---</td> </tr> </tbody> </table> | Dimension | Acceptable number | Mini. Space | $\Phi \leq 0.15$ | Ignore | --- | $0.15 < \Phi \leq 0.20$ | 3 | 5 m m | $0.20 < \Phi \leq 0.30$ | 2 | $\Phi > 0.30$ | 0 | --- | | | | | |
| | | Dimension | Acceptable number | Mini. Space | | | | | | | | | | | | | | | | | |
| | | $\Phi \leq 0.15$ | Ignore | --- | | | | | | | | | | | | | | | | | |
| | | $0.15 < \Phi \leq 0.20$ | 3 | 5 m m | | | | | | | | | | | | | | | | | |
| $0.20 < \Phi \leq 0.30$ | 2 | | | | | | | | | | | | | | | | | | | | |
| $\Phi > 0.30$ | 0 | --- | | | | | | | | | | | | | | | | | | | |
| <p>3-3 Polarizer Bubble</p> <table border="1"> <thead> <tr> <th>Dimension</th> <th>Acceptable number</th> <th>Mini. Space</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.25$</td> <td>Ignore</td> <td>---</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.35$</td> <td>3</td> <td>15 m m</td> </tr> <tr> <td>$\Phi > 0.35$</td> <td>0</td> <td>---</td> </tr> </tbody> </table> | Dimension | Acceptable number | Mini. Space | $\Phi \leq 0.25$ | Ignore | --- | $0.25 < \Phi \leq 0.35$ | 3 | 15 m m | $\Phi > 0.35$ | 0 | --- | | | | | | | | | |
| Dimension | Acceptable number | Mini. Space | | | | | | | | | | | | | | | | | | | |
| $\Phi \leq 0.25$ | Ignore | --- | | | | | | | | | | | | | | | | | | | |
| $0.25 < \Phi \leq 0.35$ | 3 | 15 m m | | | | | | | | | | | | | | | | | | | |
| $\Phi > 0.35$ | 0 | --- | | | | | | | | | | | | | | | | | | | |
| <p>Foreign Substances</p>  <p style="text-align: right;">$\Phi = (a+b)/2$</p> | | | | | | | | | | | | | | | | | | | | | |



| NO | Item | Acceptable specification | Judgment Criterion | | | |
|----|---------------------|---|--------------------|----------------------|-------------------|-------------|
| 3 | Cosmetic Inspection | 3-4 Scratch ● Sensate scratch not allowed. ● Impassive scratch as below. Unit:mm | | | | |
| | | Length | | Width | Acceptable number | Mini. space |
| | | ----- | | $W \leq 0.05$ | Ignore | 5 m m |
| | | $L \leq 3.0$ | | $0.05 < W \leq 0.08$ | 4 | |
| | | $L \leq 3.0$ | | $0.08 < W \leq 0.15$ | 3 | --- |
| | | ---- | | $0.15 < W$ | Not allowed | |
| | | $L > 3.0$ | | ---- | Not allowed | |
| | | | | | | |
| 4 | Package | 4-1 Mixed product types 4-2 Shipping q'ty should be the same as "shipping notice form" q'ty. 4-3 Outer box can't broken. | N=0 | | | |
| 5 | LCD Mura | LCD Mura according to ND 5% keep out to determine, if keep out distance at 30cm be seen by eyes is NG, otherwise will be ok if invisible. | | | | |



7. RELIABILITY

| Test Item | Test Condition |
|---|--|
| High Temperature Operation | 60°C for 96 hours |
| Low Temperature Operation | -20°C for 96 hours |
| High Temperature Storage | 70°C for 96 hours |
| Low Temperature Storage | -30°C for 96 hours |
| High Temperature Operation Humidity Operation | 60°C, 90%RH for 72 hours |
| Thermal Shock | -10°C (30min) ~ +25°C (5min) ~ +60°C (30min) for 10 cycles |
| Vibration Test (No Operation) | Frequency: 10~55Hz Amplitude:1.0mm Sweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z |
| Static electricity test | Touch 4KV, air touch 8KV |



8. HANDLING PRECAUTION

8.1 SAFETY

- (1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
- (2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
- (3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

- (1) Store the panel or module in a dark place where the temperature is $23\pm 5^{\circ}\text{C}$ and the humidity is below $50\pm 20\% \text{RH}$.
- (2) Store in anti-static electricity container.
- (3) Store in clean environment, free from dust, active gas, and solvent.
- (4) Do not place the module near organics solvents or corrosive gases.
- (5) Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

- (1) Avoid static electricity which can damage the CMOS LSI.
- (2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
- (3) Do not give external shock.
- (4) Do not apply excessive force on the surface.
- (5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- (6) Do not use ketonic solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
- (7) Do not operate it above the absolute maximum rating.
- (8) Do not remove the panel or frame from the module.

8.4 WARRANTY

- 1) The period is within twelve months since the date of shipping out under normal using and storage conditions.
- 2) According to Kingtech TFT LCD quality standard, Kingtech will rework or exchange for functional defect goods since within one year.



9. Packagingfigure

