



# PRODUCT SPECIFICATION

MODEL: PV03400AR39A- CO1

CUSTOMER NO. :

< ◆ > PRELIMINARY SPECIFICATION

< ◇ > APPROVAL SPECIFICATION

|                    |
|--------------------|
| <b>CUSTOMER</b>    |
|                    |
| <b>APPROVED BY</b> |
|                    |
| <b>DATE:</b>       |

| DESIGNED | CHECKED | APPROVED |
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|          |         |          |



## REVISION RECORD

| <u>REV NO</u> | <u>REV DATE</u> | <u>PAGE</u> | <u>CONTENTS</u> | <u>ISSUER</u> |
|---------------|-----------------|-------------|-----------------|---------------|
| 0.0           | 2023-05-17      | 14          | First Release   | Qinpingquan   |



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## 1.0 GENERAL SPECIFICATIONS

PV03400AR39A-C01 is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, FPC and a backlight unit. The module display area contains 800 \* 800 pixels. This product accords with RoHS environmental criterion.

| <b>Item</b>           | <b>Contents</b> | <b>Unit</b>       |
|-----------------------|-----------------|-------------------|
| Screen Diagonal       | 3.4"            | Inch              |
| Viewing direction     | Free            |                   |
| Number of Dots        | 800(RGB) * 800  | /                 |
| Display Mode          | Normally Black  | /                 |
| Number of color       | 16.7M           | /                 |
| outline dimension     | 96.6* 99* 3.98  | mm                |
| Active area           | Φ 87.6          | mm                |
| Interface             | MIPI            |                   |
| CTP Driver IC         | CF1133          |                   |
| LCM Luminance         | 320(typ)        | cd/m <sup>2</sup> |
| Response Time (Tr+Tf) | 25ms (typ)      | /                 |



## 2.0 ABSOLUTE MAXIMUM RATINGS

The following are maximum values which if exceeded may cause faulty operation or damage to the unit.

| Item                  | Symbol   | Values |      | Unit | Remark |
|-----------------------|----------|--------|------|------|--------|
|                       |          | Min.   | Max. |      |        |
| Power Supply Voltage  | VDD(+5V) | -0.3   | 6.5  | V    |        |
| Power Supply Voltage  | VDD(-5V) | -6.5   | +0.3 | V    |        |
| Power Supply Voltage  | IOVCC    | -0.3   | 3.3  | V    |        |
| Operation Temperature | TOP      | -20    | 70   | °C   |        |
| Storage Temperature   | TST      | -30    | 80   | °C   |        |

## 3.0 ELECTRICAL CHARACTERISTICS

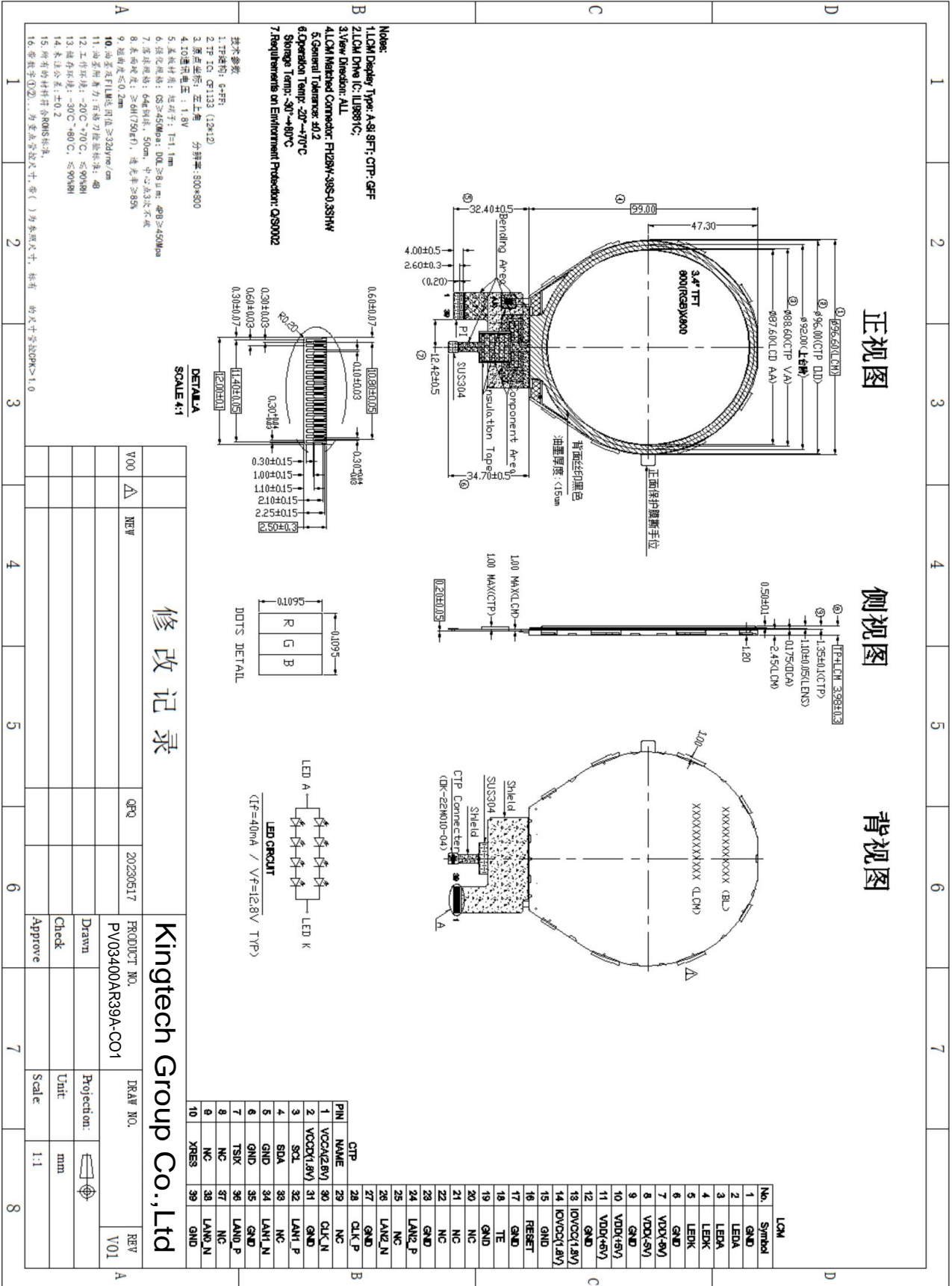
| Item                           | Symbol   | Values    |      |            | Unit | Remark |
|--------------------------------|----------|-----------|------|------------|------|--------|
|                                |          | Min.      | Typ. | Max.       |      |        |
| Logic Operating Voltage        | IOVCC    | 1.7       | 1.8  | 1.9        | V    |        |
| Positive source output voltage | VDD(+5V) | 4.9       | 5    | 5.1        | V    |        |
| Negative source output voltage | VDD(-5V) | -5.1      | -5   | -4.9       | V    |        |
| Input Signal Voltage           | VIH      | 0.7*IOVCC | -    | IOVCC      | V    |        |
| Input Signal Voltage           | VIL      | 0         | -    | 0.3* IOVCC | V    |        |

## 3.1 BACKLIGHT CHARACTERISTICS

| Item            | Symbol | Min    | Typ | Max | Unit              | Condition |
|-----------------|--------|--------|-----|-----|-------------------|-----------|
| Forward voltage | Vf     | 2.9    | 3.2 | 3.4 | V                 | If = 40mA |
| Luminance       | Lv     | 270    | 320 | --  | cd/m <sup>2</sup> | If = 40mA |
| Number of LED   | --     | 2*4pcs |     |     | Piece             | --        |



4.0 DIMENSIONAL DRAWING





## 5.0 PINTERFACE PIN CONNECTIONS

LCM pin

Matched connector:DF30FC-34DP-0.4V

| Pin No. | Symbol   | Function                                  |
|---------|----------|---|
| 1       | GND      | Ground                                    |
| 2       | LEDA     | Power for LED backlight (Anode)           |
| 3       | LEDA     | Power for LED backlight (Anode)           |
| 4       | LEDK     | Power for LED backlight (Cathode)         |
| 5       | LEDK     | Power for LED backlight (Cathode)         |
| 6       | GND      | Ground                                    |
| 7       | VDD(-5V) | -5v INPUT                                 |
| 8       | VDD(-5V) | -5v INPUT                                 |
| 9       | GND      | Ground                                    |
| 10      | VDD(+5V) | +5v INPUT                                 |
| 11      | VDD(+5V) | +5v INPUT                                 |
| 12      | GND      | Ground                                    |
| 13      | IOVCC    | Power supply 1.8v                         |
| 14      | IOVCC    | Power supply 1.8v                         |
| 15      | GND      | Ground                                    |
| 16      | RESET    | Global reset pin                          |
| 17      | GND      | Ground                                    |
| 18      | TE       | Serve as a TE(tearing Fffer)output signal |
| 19      | GND      | Ground                                    |
| 20      | NC       | No connection                             |
| 21      | NC       | No connection                             |
| 22      | NC       | No connection                             |
| 23      | GND      | Ground                                    |
| 24      | LAN2_P   | MIPI D2p data input                       |
| 25      | NC       | No connection                             |
| 26      | LAN2_N   | MIPI D2N data input                       |
| 27      | GND      | Ground                                    |
| 28      | CLK_P    | MIPI CLKP data input                      |
| 29      | NC       | No connection                             |
| 30      | CLK_N    | MIPI CLKN data input                      |
| 31      | GND      | Ground                                    |



|    |        |                     |
|----|--------|---------------------|
| 32 | LAN1_P | MIPI D1P data input |
| 33 | NC     | No connection       |
| 34 | LAN1_N | MIPI D1N data input |
| 35 | GND    | Ground              |
| 36 | LAN0_P | MIPI D0P data input |
| 37 | NC     | No connection       |
| 38 | LAN0_N | MIPI D0N data input |
| 39 | GND    | Ground              |

## TP PIN

|           |            |                             |
|-----------|------------|-----------------------------|
| <b>1</b>  | VCCA(2.8V) | Power supply 2.8v           |
| <b>2</b>  | VCCD(1.8V) | Power supply 1.8v           |
| <b>3</b>  | SCL        | clock for CTP IIC interface |
| <b>4</b>  | SDA        | Data for CTP IIC interface  |
| <b>5</b>  | GND        | Ground                      |
| <b>6</b>  | GND        | Ground                      |
| <b>7</b>  | TSIX       | TP interrupt for CTP        |
| <b>8</b>  | NC         | No connection               |
| <b>9</b>  | NC         | No connection               |
| <b>10</b> | XRES       | TP reset pin                |



## 6.0 TIMING CHARACTERISTICS OF INPUT SIGNAL

Please refer to (Driver IC) datasheet

### 5.1 LCM Timing

#### 5.1.1 Reset timing characteristics

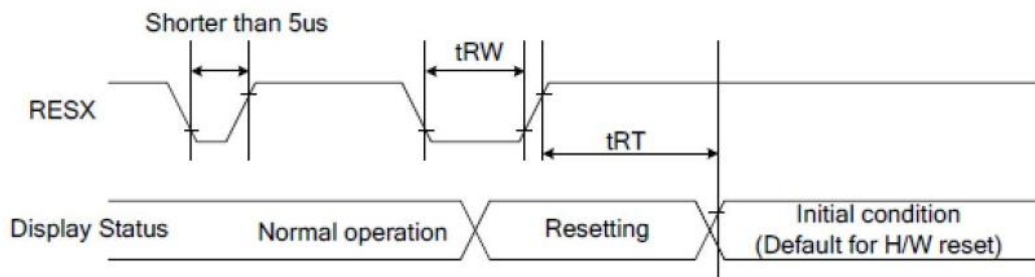


Figure 124: Reset Timing

Table 47: Reset Timing

| Signal | Symbol | Parameter            | Min | Max                              | Unit |
|--------|--------|----------------------|-----|----------------------------------|------|
| RESX   | tRW    | Reset pulse duration | 10  |                                  | uS   |
|        | tRT    | Reset cancel         |     | 5 (note 1,5)<br>120 (note 1,6,7) | mS   |

**Notes:**

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

Table 48: Reset Descript

| RESX Pulse           | Action         |
|----------------------|----------------|
| Shorter than 5us     | Reset Rejected |
| Longer than 10us     | Reset          |
| Between 5us and 10us | Reset starts   |

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

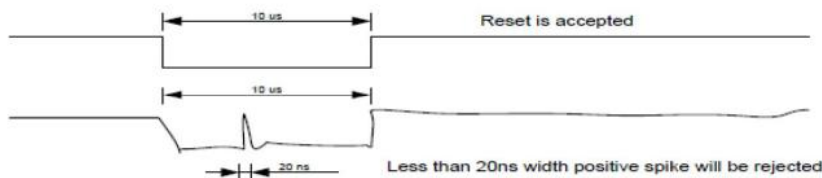


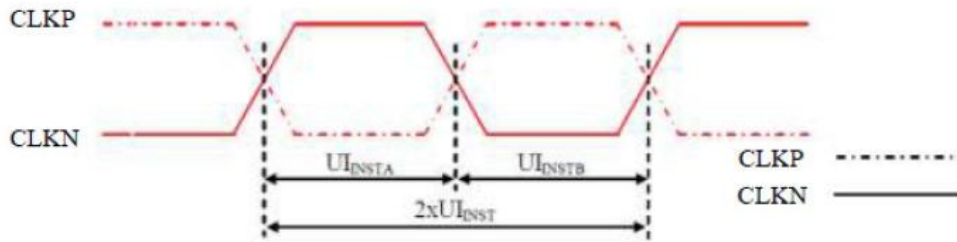
Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



**5.1.2 High Speed Mode**

**18.4.2. High Speed Mode – Clock Channel Timing**



**Figure 116: DSI Clock Channel Timing**

**Table 38: DSI Clock Channel Timing**

| Signal | Symbol                               | Parameter               | Min    | Max  | Unit |
|--------|--------------------------------------|-------------------------|--------|------|------|
| CLKP/N | $2xUI_{INST}$                        | Double UI instantaneous | Note 2 | 25   | ns   |
| CLKP/N | $UI_{INSTA}, UI_{INSTB}$<br>(Note 1) | UI instantaneous Half   | Note 2 | 12.5 | ns   |

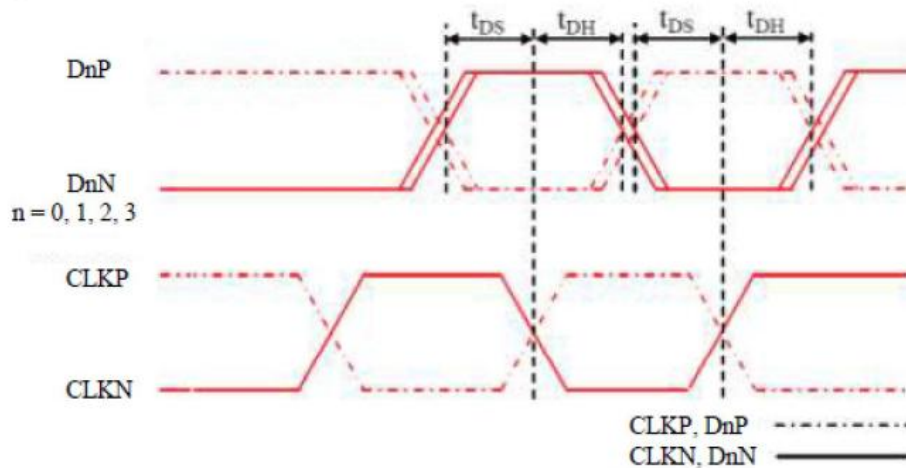
**Notes:**

1.  $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value, see Table 39.

**Table 39: Limited Clock Channel Speed**

| Data type   | Two Lanes speed | Three Lanes speed | Four Lanes speed |
|---|-----------------|-------------------|------------------|
| Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel         | 566 Mbps        | 466 Mbps          | 366 Mbps         |
| Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel         | 637 Mbps        | 525 Mbps          | 412 Mbps         |
| Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel | 850 Mbps        | 700 Mbps          | 550 Mbps         |
| Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel         | 850 Mbps        | 700 Mbps          | 550 Mbps         |

**18.4.3. High Speed Mode – Data Clock Channel Timing**



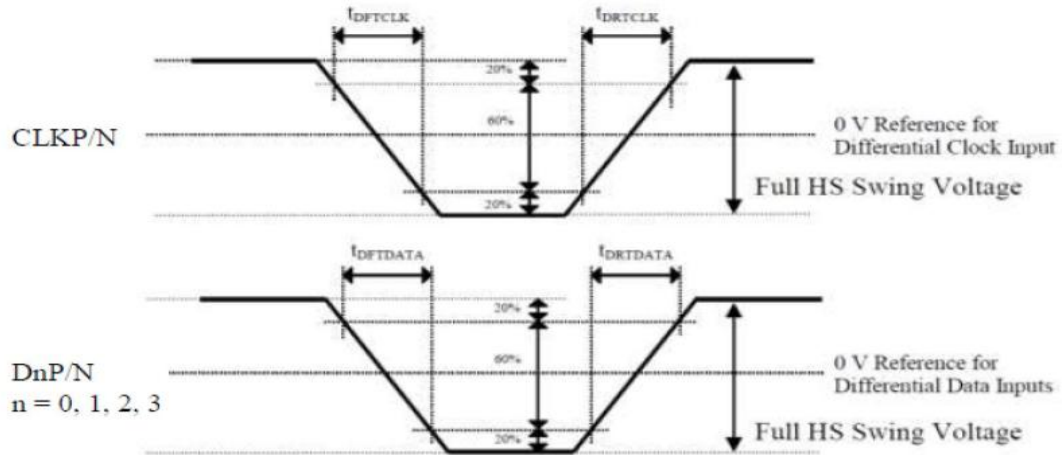
**Figure 117: DSI Data to Clock Channel Timings**

**Table 40: DSI Data to Clock Channel Timings**

| Signal           | Symbol   | Parameter                | Min       | Max |
|------------------|----------|--------------------------|-----------|-----|
| DnP/N, n=0 and 1 | $t_{DS}$ | Data to Clock Setup time | $0.15xUI$ | -   |
|                  | $t_{DH}$ | Clock to Data Hold Time  | $0.15xUI$ | -   |



**18.4.4. High Speed Mode – Rising and Falling Timings**



**Figure 118: Rising and Falling Timings on Clock and Data Channels**

**Table 41: Rise and Fall Timings on Clock and Data Channels**

| Parameter                        | Symbol        | Condition          | Specification |     |              |
|----------------------------------|---------------|--------------------|---------------|-----|--------------|
|                                  |               |                    | Min           | Typ | Max          |
| Differential Rise Time for Clock | $t_{DRTCLK}$  | CLKP/N             | 150 ps        | -   | 0.3UI (Note) |
| Differential Rise Time for Data  | $t_{DRTDATA}$ | DnP/N<br>n=0 and 1 | 150 ps        | -   | 0.3UI (Note) |
| Differential Fall Time for Clock | $t_{DFTCLK}$  | CLKP/N             | 150 ps        | -   | 0.3UI (Note) |
| Differential Fall Time for Data  | $t_{DFTDATA}$ | DnP/N<br>n=0 and 1 | 150 ps        | -   | 0.3UI (Note) |

**Note:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.



## 7.0 ELECTRO-OPTICAL CHARACTERISTICS

Ta=25°C

| ITEM                                 |            | SYMBOL     | CONDITION          | MIN.  | TYP.  | MAX.  | UNIT              | NOTE  |
|--------------------------------------|------------|------------|--------------------|-------|-------|-------|-------------------|-------|
| Luminance                            |            | Lv         | $\theta = 0^\circ$ | 270   | 320   | --    | cd/m <sup>2</sup> | Note1 |
| Contrast Ratio                       |            | CR         | $\theta = 0^\circ$ | 600   | 800   | --    | -                 | Note3 |
| Response Time                        |            | Rr+Tf      | $\theta = 0^\circ$ | --    | 25    | 35    | ms                | Note4 |
| Viewing Angle<br>K=Contrast Ratio>10 | Horizontal | $\Theta_L$ | CR>100<br>= 25°    | 70    | 80    | --    |                   | Note2 |
|                                      |            | $\Theta_R$ |                    | 70    | 80    | --    |                   |       |
|                                      | Vertical   | $\Theta_U$ |                    | 70    | 80    | --    |                   |       |
|                                      |            | $\Theta_D$ |                    | 70    | 80    | --    |                   |       |
|                                      |            | Y          |                    | 0.282 | 0.322 | 0.362 |                   |       |
| Color gamut (NTSC ratio)             |            |            |                    | 70    | 80    | -     | %                 |       |

Test Conditions:

1. VDD=2.5V, the ambient temperature is 25°C.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

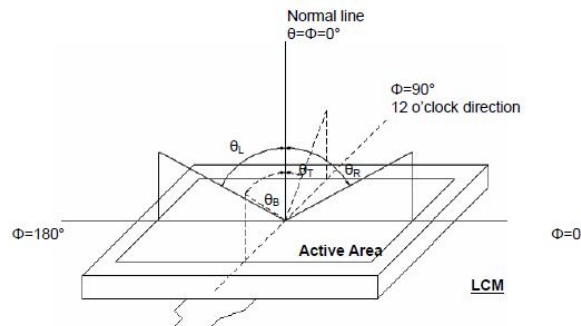


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1° /Height: 500mm.)

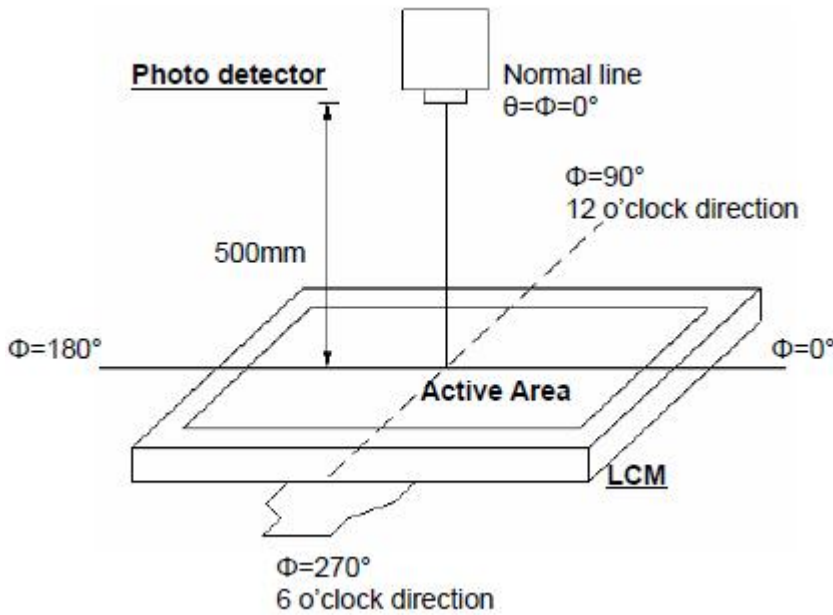


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

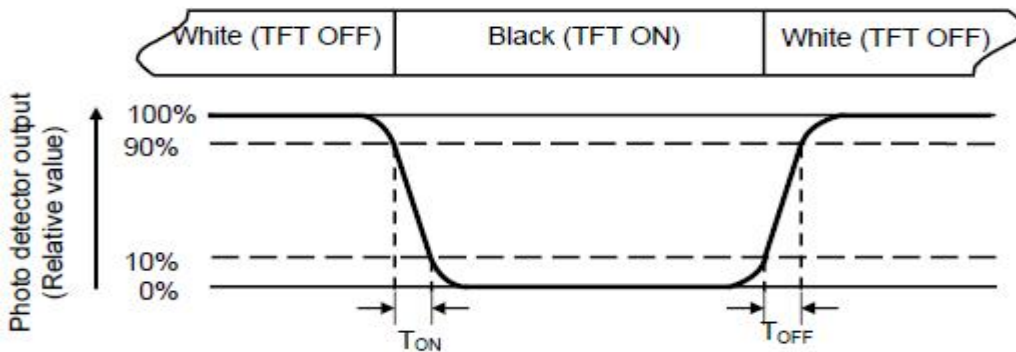


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

Luminance measured when LCD on the "Black" state

Luminance measured when LCD on the "White" state

Contrast ratio (CR) =

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IF=40mA .

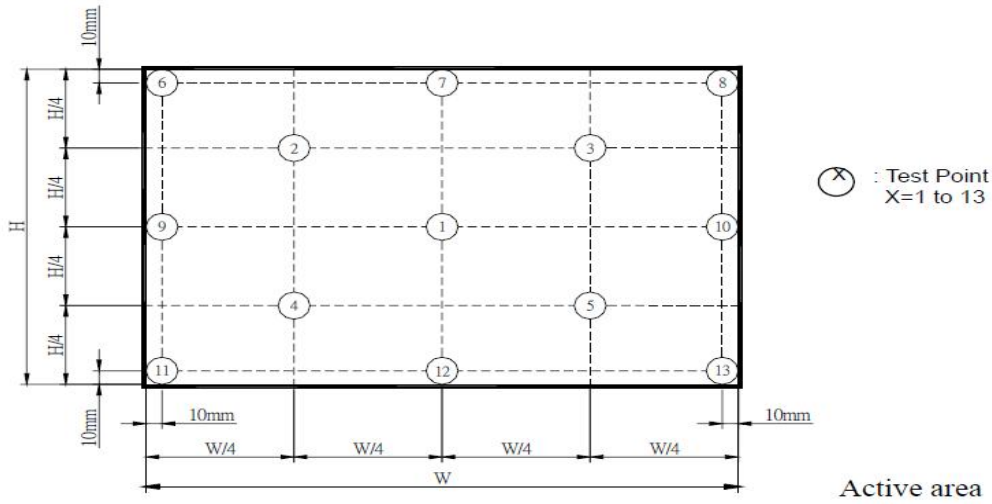
Note 7: Definition of Luminance Uniformity



Measure the luminance of gray level 63 at 9 points

$$\delta W9p = \{ \text{Minimum} [L(1) + L(6) + L(7) + L(8) + L(9) + L(10) + L(11) + L(12) + L(13)] /$$

$$\text{Maximum} [L(1) + L(6) + L(7) + L(8) + L(9) + L(10) + L(11) + L(12) + L(13)] \} * 100\%$$





## 8.0 RELIABILITY

### 8.1 MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

### 8.2 Tests

| NO. | Test Item  | Test condition   | Criterion   |
|-----|--|--|---|
| 1   | High Temperature Storage                         | 80°C±2°C 96H<br>Restore 24H at 25°C<br>Power off                                       |   |
| 2   | Low Temperature Storage                          | -30°C±2°C 96H<br>Restore 24H at 25°C<br>Power off                                      |   |
| 3   | High Temperature Operation                       | 70°C±2°C 96H<br>Restore 24H at 25°C<br>Power on  |   |
| 4   | Low Temperature Operation                        | -20°C±2°C 96H<br>Restore 24H at 25°C<br>Power on                                       |   |
| 5   | High Temperature & Humidity Operation            | 60°C±2°C 90%RH 96H<br>Power on   |   |
| 6   | Temperature Cycle                                | -10°C↔25°C↔60°C<br>30min 5min 30min<br>after 10cycle, Restore 24H at<br>25°C Power off | Aftertesting,cosmetic<br>and electrical defects<br>should not happen. |
| 7   | Vibration Test                                   | 10Hz~45Hz, 100m/s2, 120min   |   |
| 8   | Electro Static Discharge Test<br>(non-operation) | 150pF, 330Ω, Contact:±<br>4KV,Air:±8KV<br>Measure point :LCD glass and<br>metal bezel  | IEC61000-4-2: 2001<br>GB/T17626.2-2006                                |

## 9.0 HANDLING PRECAUTION

- (1) Don't disassemble and reassemble the module by self.
- (2) Acid, alkali, alcohol or touched directly by hand will damage the display.
- (3) Static electricity will damage the module. Please configure grounding device.
- (4) The strong vibration, shock, twist or bend will cause material damage, even module broken.
- (5) It is easy to cause image sticking while displaying the same pattern for very long time.
- (6) The response time, brightness and performance will vary from different temperature.