



SPECIFICATION

Product Model: PV028000YX50D-R

V00

Designed by	R&D Checked by	Quality Department by	Approved by

Approval by Customer

<p>OK</p> <p>NG, Problem survey:</p> <p>Approved By _____</p>



Table Of Contents

List	Description	Page No.
	Cover	1
	Revision Record	2
	Table Of Contents	3
1	Numbering System	4
2	General Information	4
3	External Dimensions	5
4	Interface Description	6
5	Absolute Maximum Ratings	7
6	Electrical Characteristics	7
7	Timing Characteristics	8
8	Backlight Characteristics	11
9	Optical Characteristics	11
10	Reliability Test Conditions And Methods	14
11	Inspection Standard	15
12	Handling Precautions	18
13	Precaution For Use	19
14	Packing Method	19



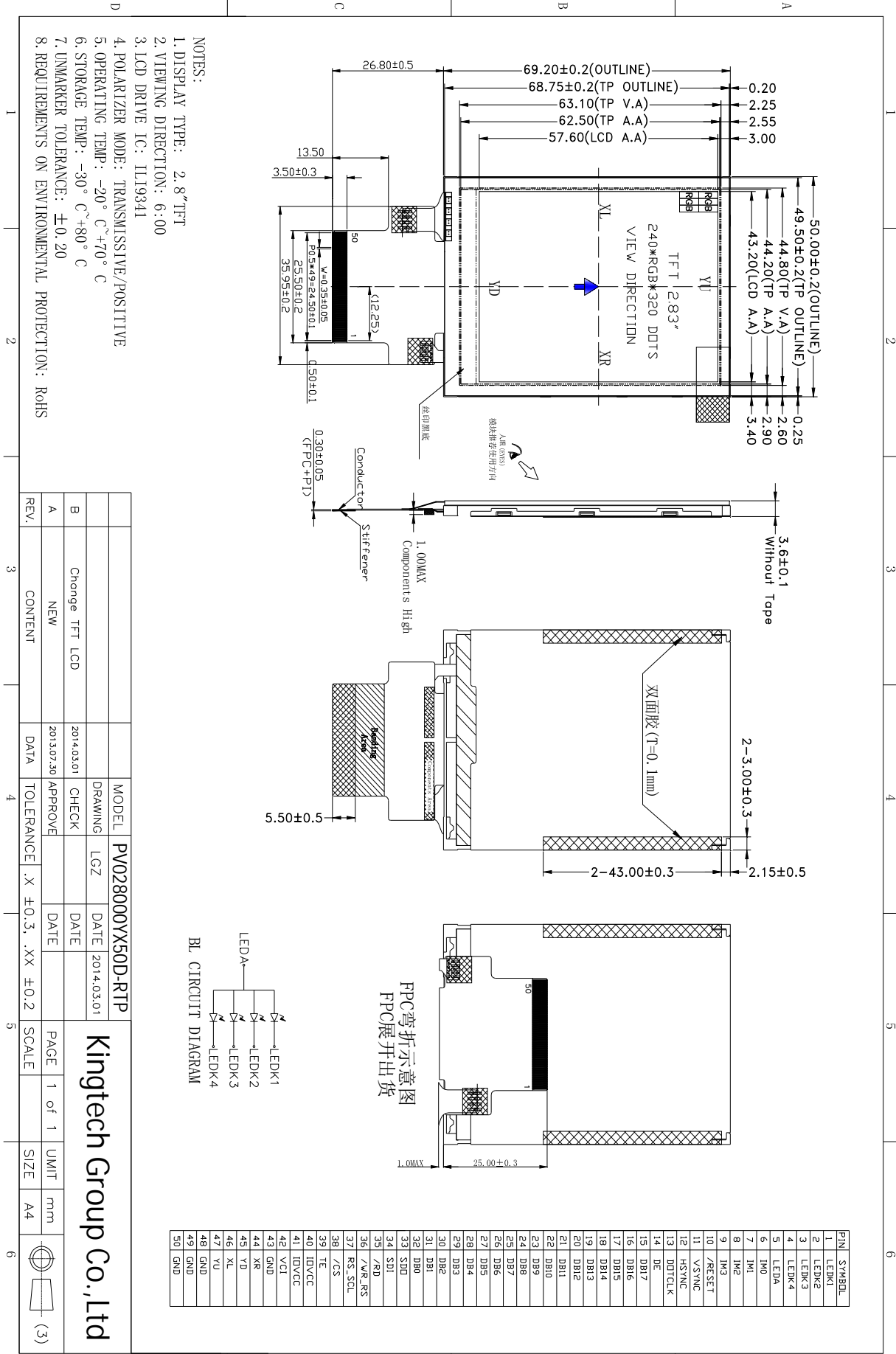
1. Numbering System

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	2.8" TFT	--
Dot arrangement	240(RGB)×320	dots
Color filter array	RGB vertical stripe	--
Display mode	TN / Transmission / Normally White	--
Viewing Direction	6 o'clock	--
Driver IC	ILI9341	--
Module size	50.0(W)×69.2(H)×3.6(T)	mm
Active area	43.2(W)×57.6(H)	mm
Dot pitch	0.18(W)×0.18(H)	mm
Interface	4-lines_8bit / 3-lines_9bit SPI 8-/9-/16-/18-bit 8080-series system interface 6-/16-/18-bit RGB interface	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	4 White LED In Parallel	--
Weight	TBD	g



3. External Dimensions



Kingtech Group Co., Ltd

REV.	CONTENT	DATE	APPROVE	TOLERANCE	SCALE	UNIT	SIZE
A	NEW	2013.07.30		X ±0.3, .XX ±0.2		mm	A4
B	Change TFT LCD	2014.03.01	CHECK				

MODEL	DATE	DATE
PV028000YX50D-RTP	2014.03.01	

LGZ	DATE
	2014.03.01

DATE	SCALE
	1 of 1

DATE	SCALE
	(3)



4. Interface Description

Pin	Symbol	Description.																																																																														
1	LEDK1	LED backlight (Cathode).																																																																														
2	LEDK2	LED backlight (Cathode).																																																																														
3	LEDK3	LED backlight (Cathode).																																																																														
4	LEDK4	LED backlight (Cathode).																																																																														
5	LEDA	LED backlight (Anode).																																																																														
6	IM0	System interface Mode																																																																														
		<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>Interface mode</th> <th>DB Pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>i80-system 8-bit interface I</td> <td>DB[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>i80-system 16-bit interface I</td> <td>DB[15:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 9-bit interface I</td> <td>DB[8:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 18-bit interface I</td> <td>DB[17:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wires_9-bit SPI I</td> <td>/CS,SDI,SCL</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wires_8-bit SPI I</td> <td>/CS,RS,SDI,SCL</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>i80-system 16-bit interface II</td> <td>DB[17:10],DB[8:1]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>i80-system 8-bit interface II</td> <td>DB[17:10]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 18-bit interface II</td> <td>DB[17:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 9-bit interface II</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wires_9-bit SPI II</td> <td>/CS,SDI,SDO,SCL</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wires_8-bit SPI II</td> <td>/CS,RS,SDI,SDO,SCL</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	Interface mode	DB Pin	0	0	0	0	i80-system 8-bit interface I	DB[7:0]	0	0	0	1	i80-system 16-bit interface I	DB[15:0]	0	0	1	0	i80-system 9-bit interface I	DB[8:0]	0	0	1	1	i80-system 18-bit interface I	DB[17:0]	0	1	0	1	3-wires_9-bit SPI I	/CS,SDI,SCL	0	1	1	0	4-wires_8-bit SPI I	/CS,RS,SDI,SCL	1	0	0	0	i80-system 16-bit interface II	DB[17:10],DB[8:1]	1	0	0	1	i80-system 8-bit interface II	DB[17:10]	1	0	1	0	i80-system 18-bit interface II	DB[17:0]	1	0	1	1	i80-system 9-bit interface II	DB[17:9]	1	1	0	1	3-wires_9-bit SPI II	/CS,SDI,SDO,SCL	1	1	1	0	4-wires_8-bit SPI II	/CS,RS,SDI,SDO,SCL
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7	IM1																																																																															
8	IM2																																																																															
9	IM3																																																																															
10	/RESET	Reset input pin, Active "L".																																																																														
11	VSYNC	Vertical sync signal in RGB I/F.																																																																														
12	HSYNC	Horizontal sync signal in RGB I/F.																																																																														
13	DOTCLK	Pixel clock signal in RGB I/F.																																																																														
14	DE	Data enable signal in RGB I/F mode																																																																														
15	DB17	16-bit parallel bi-directional data bus for MPU- I system: 8-bit I/F: DB[7:0] is used. 9-bit I/F: DB[8:0] is used. 16-bit I/F: DB[15:0] is used. 18-bit I/F: DB[17:0] is used.																																																																														
16	DB16																																																																															
17	DB15																																																																															
18	DB14																																																																															
19	DB13																																																																															
20	DB12																																																																															
21	DB11																																																																															
22	DB10	18-bit parallel bi-directional data bus for MPU- II system: 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used.																																																																														
23	DB9																																																																															
24	DB8																																																																															
25	DB7																																																																															
26	DB6	18-bit input data bus for RGB I/F. 6-bit/pixel: DB[5:0] is used; 16-bit/pixel: DB[17:13]=R[4:0], DB[11:6]=G[5:0] and DB[5:1]=B[4:0]; 18-bit/pixel: DB[17:12]=R[5:0], DB[11:6]=G[5:0] and DB[5:0]=B[5:0]; Connect unused pins to GND.																																																																														
27	DB5																																																																															
28	DB4																																																																															
29	DB3																																																																															
30	DB2																																																																															
31	DB1																																																																															
32	DB0																																																																															
33	SDO	Serial output signal in SPI I/F.																																																																														



34	SDI	Serial input signal in SPI I/F.
35	/RD	Reads strobe signal to write data when /RD is "Low" in MPU interface.
36	/WR_RS	MCU: Serves as a write signal and writes data at the rising edge. 4-line SPI: Serves as command or parameter select.
37	RS_SCL	Display data / command selection in 80-series MPU I/F. RS = "0" : Command RS = "1" : Display data. SPI: This pin is used serial interface clock in SPI.
38	/CS	Chip select input pin ("Low" enable) in MPU I/F and SPI I/F.
39	TE	Tearing effect output pin to synchronize MPU to frame writing.
40	IOVCC	I/O power supply.
41	IOVCC	I/O power supply.
42	VCI	System power supply.
43	GND	Power ground
44	XR	TOUCH PIN.
45	YD	
46	XL	
47	YU	
48	GND	Power ground
49	GND	Power ground
50	GND	Power ground

5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	IOVCC	-0.3	4.6	V
Analog Supply Voltage	VCI	-0.3	4.6	V
Input Voltage	V _{in}	-0.3	IOVCC+0.3	V
Operating Temperature	T _{OP}	-20	70	°C
Storage Temperature	T _{ST}	-30	80	°C
Storage Humidity	HD	20	90	%RH

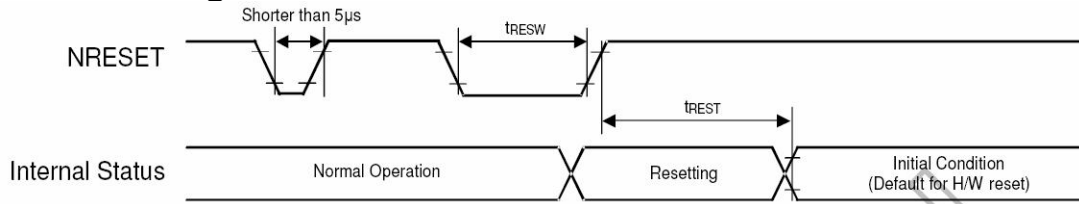
6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	1.8/2.8	3.3	V	-
Analog Supply Voltage	VCI	2.5	2.8	3.3	V	-
Input High Voltage	V _{IH}	0.7IOVCC	-	IOVCC	V	Digital input pins
Input Low Voltage	V _{IL}	GND	-	0.3IOVCC	V	Digital input pins
Output High Voltage	V _{OH}	0.8IOVCC	-	IOVCC	V	Digital output pins
Output Low Voltage	V _{OL}	GND	-	0.2IOVCC	V	Digital output pins
I/O Leak Current	I _{LI}	-0.1	-	0.1	uA	-



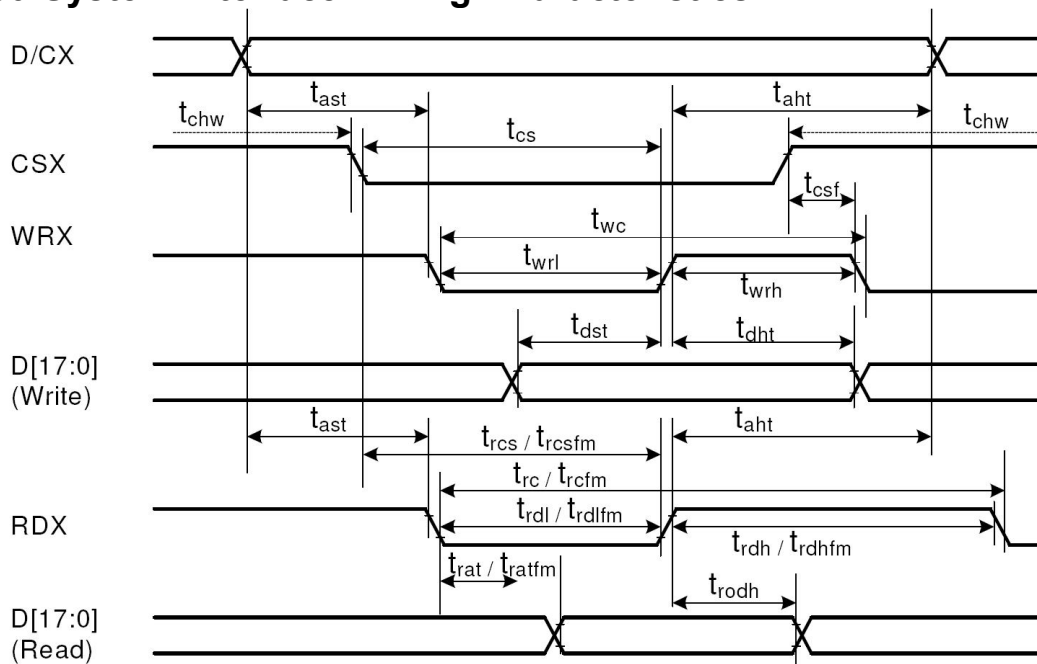
7. Timing Characteristics

7.1 Reset Timing Characteristics



Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	µs
tREST	Reset complete time ⁽²⁾	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

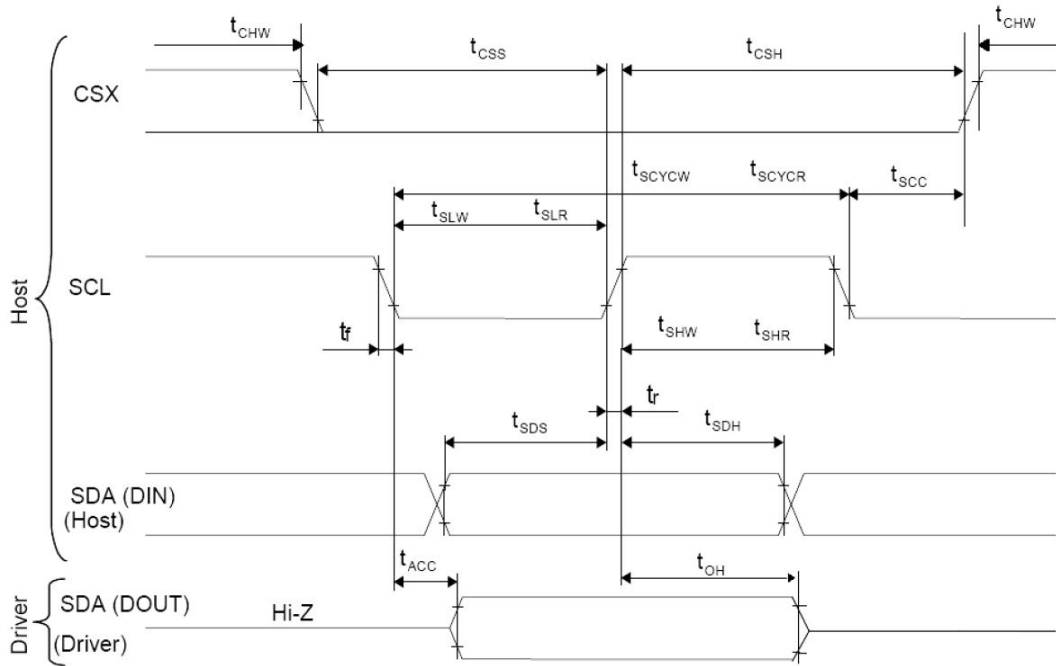
7.2 i80-System Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{aht}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{trcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{trcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{trcfm}	Read Cycle (FM)	450	-	ns	
	t _{trdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{trdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{trc}	Read cycle (ID)	160	-	ns	
	t _{trdh}	Read Control pulse H duration	90	-	ns	
	t _{trdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time (FM)	-	340	ns	
	t _{rodh}	Read output disable time	20	80	ns	

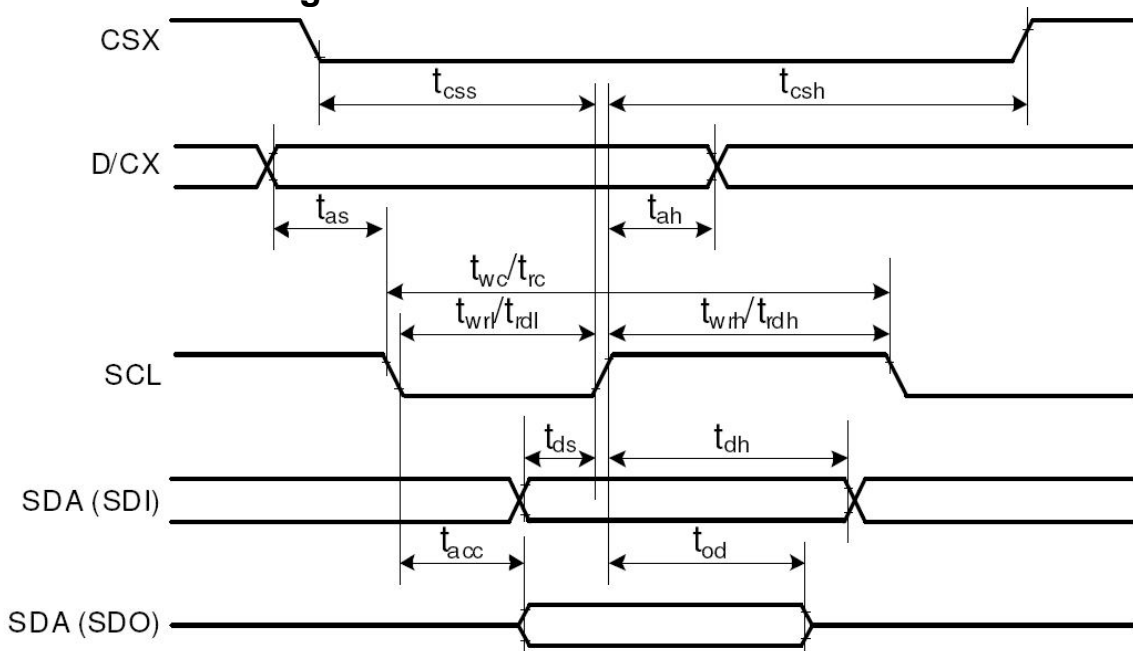


7.3 3-line SPI Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscyrc	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcs		65	-	ns	

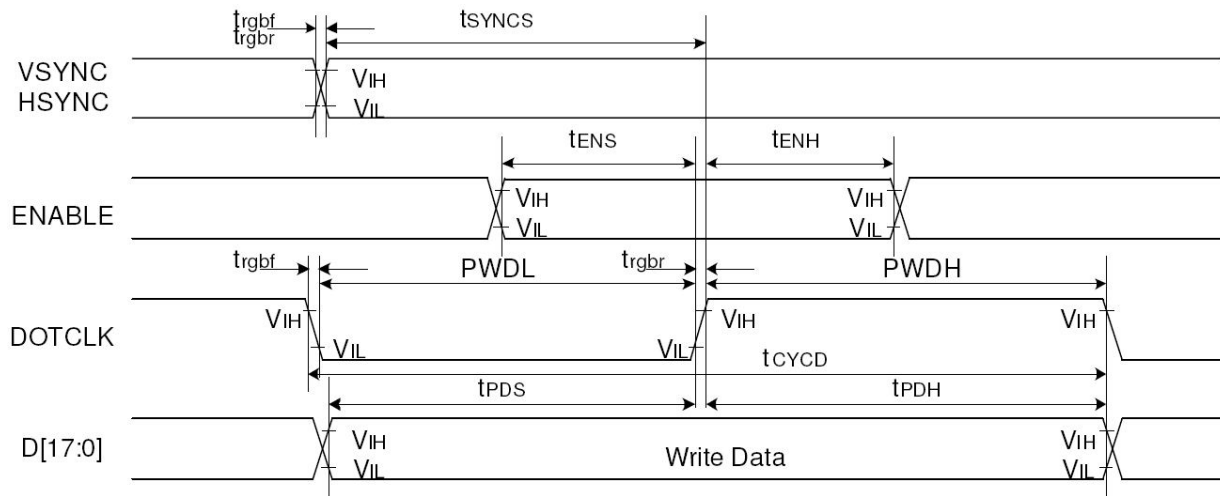
7.4 4-line SPI Timing Characteristics





Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

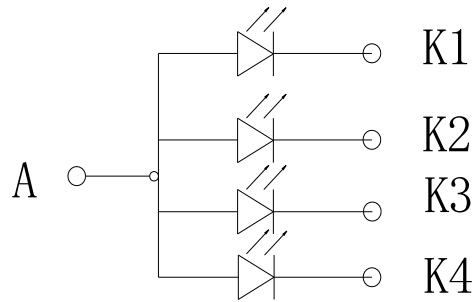
7.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description	
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode	
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns		
DE	tENS	DE setup time	15	-	ns		
	tENH	DE hold time	15	-	ns		
D[17:0]	tPOS	Data setup time	15	-	ns		
	tPDH	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns		
	PWDL	DOTCLK low-level period	15	-	ns		
	tCYCD	DOTCLK cycle time	100	-	ns		
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns		6-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns		
DE	tENS	DE setup time	15	-	ns		
	tENH	DE hold time	15	-	ns		
D[17:0]	tPOS	Data setup time	15	-	ns		
	tPDH	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns		
	PWDL	DOTCLK low-level pulse period	15	-	ns		
	tCYCD	DOTCLK cycle time	100	-	ns		
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		



8. Backlight Characteristics



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	2.9	3.2	3.5	V	If=60mA
Supply Current	If	-	60	80	mA	-
Luminous Intensity for LCM	-	200	230	-	Cd/m ²	If=60mA
Uniformity for LCM	-	80	-	-	%	If=60mA
Life Time	-	20000	-	-	Hr	If=60mA
Backlight Color	White					

9. Optical Characteristics

Item	Conditions	Min.	Typ.	Max.	Unit	Note	
Viewing Angle (CR>10)	Horizontal	θ_{x+}	-	(45)	-	degree	(1),(2),(6),(7),(8)
		θ_{x-}	-	(45)	-		
	Vertical	θ_{y+}	-	(50)	-		
		θ_{y-}	-	(20)	-		
Contrast Ratio	Center	TBD	(500)	-	-	(1),(3),(6)(7),(8)	
Response Time	Rising + Falling	-	(16)	-	ms	(1),(4),(6),(7),(8)	
CF Color Chromaticity (CIE1931)	Red x	Typ. -0.15	(0.626)	Typ. +0.15	-	Under C-light	
	Red y		(0.336)		-		
	Green x		(0.276)		-		
	Green y		(0.550)		-		
	Blue x		(0.144)		-		
	Blue y		(0.130)		-		
	White x		(0.307)		-		
White y	(0.329)	-					
NTSC	CIE1931	-	(55.3)	-	%	(1),(6),(7),(8)	
Transmittance	-	-	(6.13)	-	%	(1),(5),(6),(7),(8)	

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25°C) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

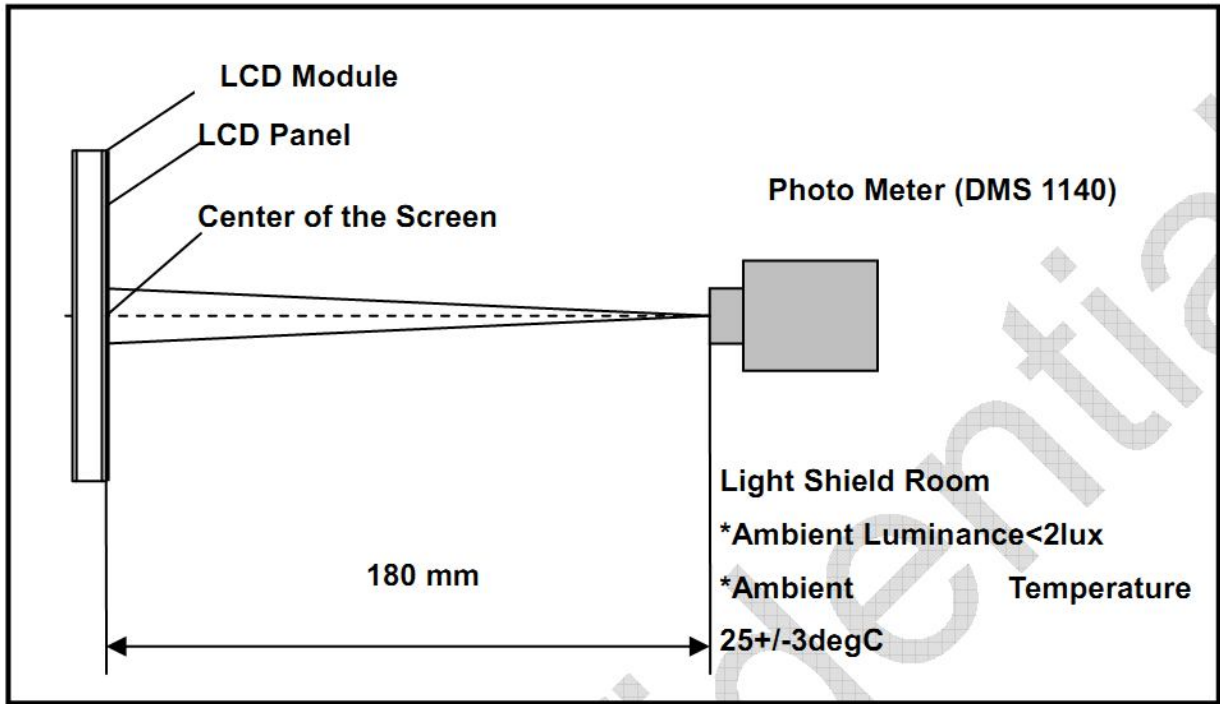


Figure 2 Measurement Setup

Note (2) Definition of Viewing Angle

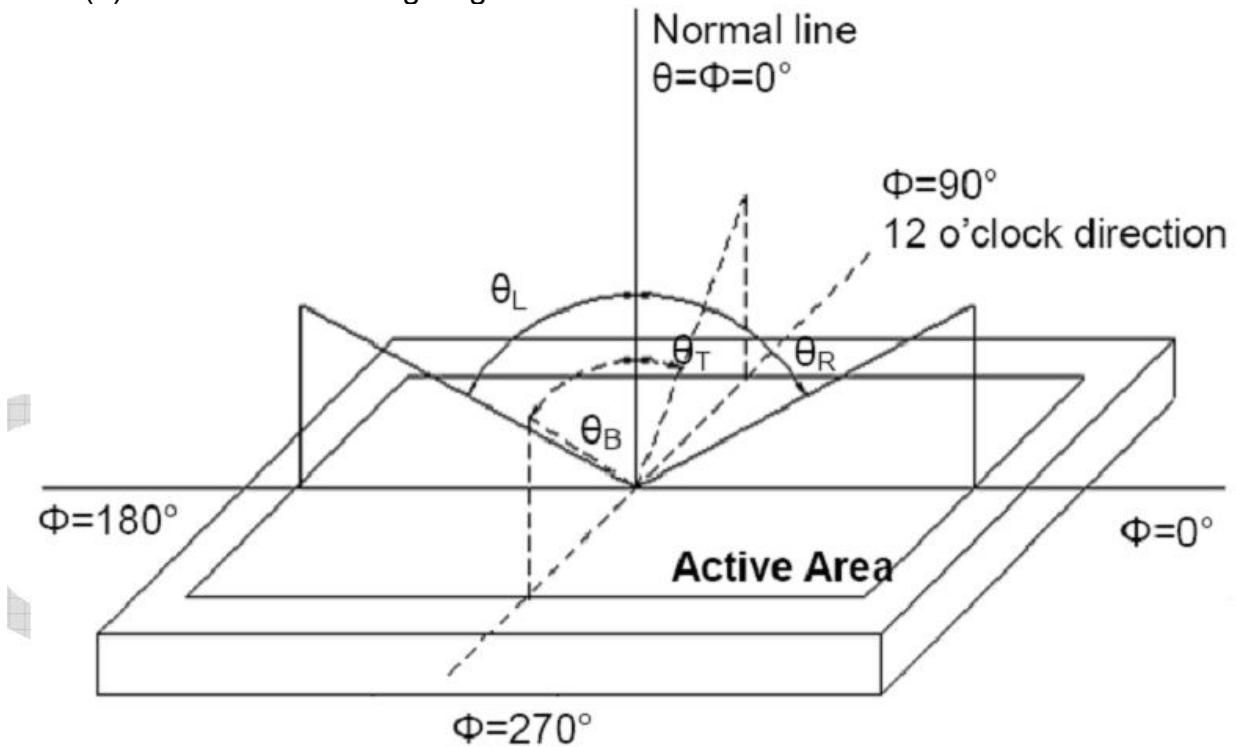


Figure 3 Definition of Viewing Angle

Note (3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition Of Response Time

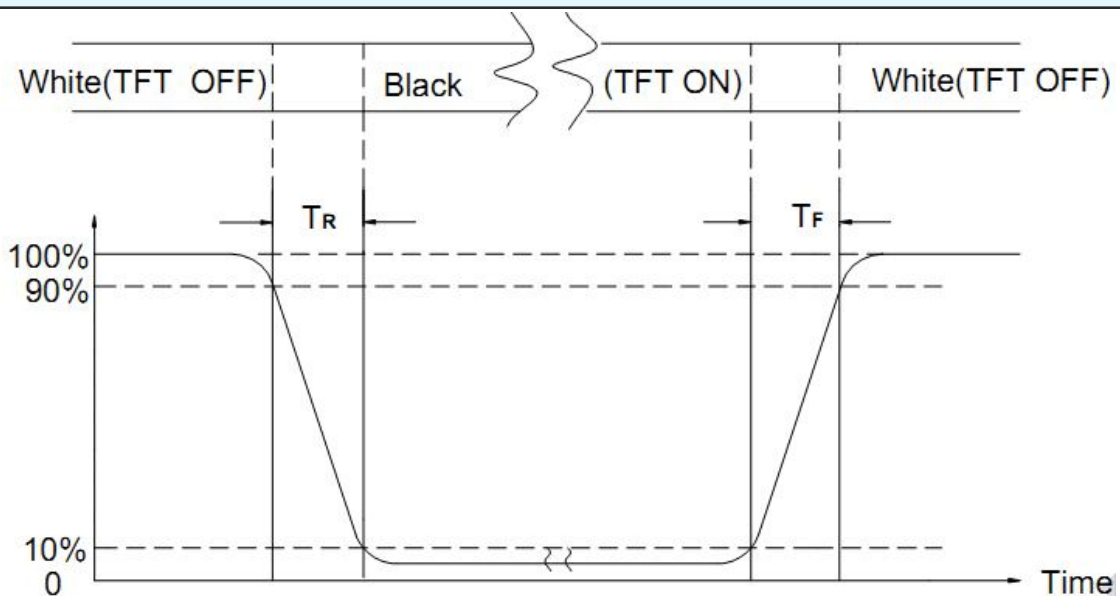


Figure 4 Definition of Response Time

Note (5) Definition of Transmittance(Module is without signal input)

Transmittance = (Center Luminance of LCD / Center Luminance of Back Light) X 100%

Note (6) Light source is the BLU which is supplied by IVO.

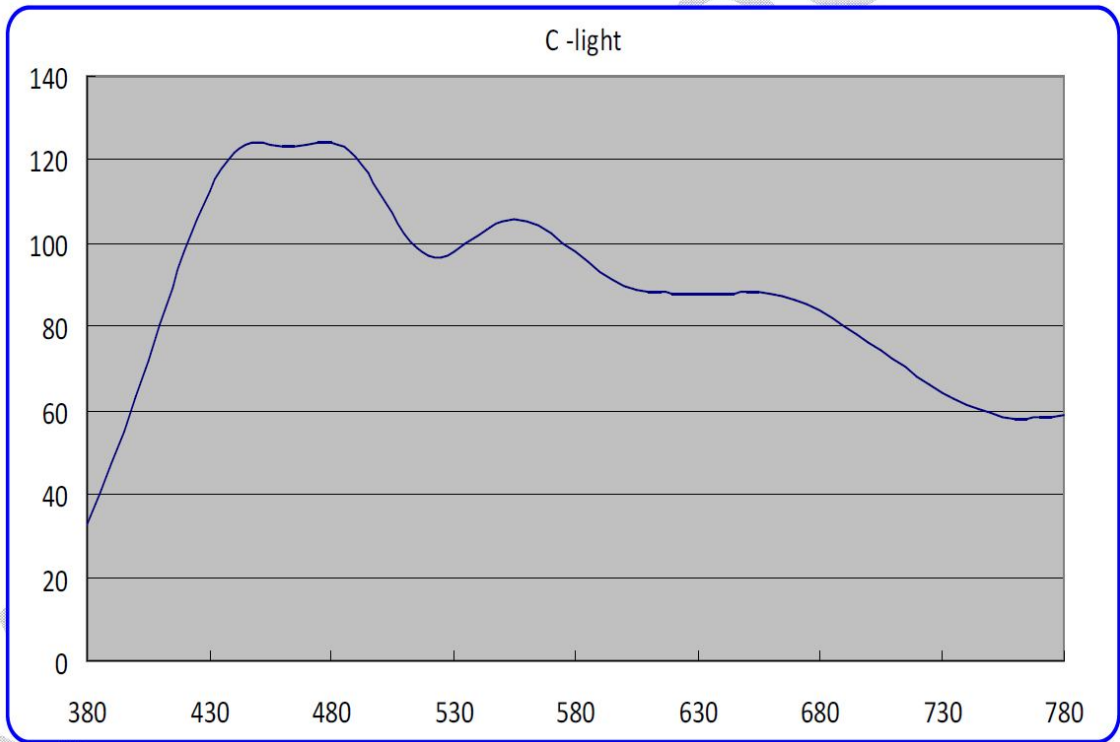


Figure 5 Back Light Spectrum

Note (7) The polarizer type: TBD/CF, TBD/Array.

Note (8) All optical data based on IVO given polarizer & Backlight& testing machine in this document.



10. Reliability Test Conditions And Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
①	High Temperature Storage	80°C±2°C×200Hours	Inspection after 2~4hours storage at room temperature,the samples should be free from defects: 1,Air bubble in the LCD. 2,Sealleak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7,The surface shall be free from damage. 8,The electric charateristic requirements shall be satisfied.
②	Low Temperature Storage	-30°C±2°C×200Hours	
③	High Temperature Operating	70°C±2°C×120Hours	
④	Low Temperature Operating	-20°C±2°C×120Hours	
⑤	Temperature Cycle(Storage)	-20°C ↔ 25°C ↔ 70°C (30min) (5min) (30min) 1cycle Total 10cycle	
⑥	Damp Proof Test (Storage)	50°C±5°C×90%RH×120Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
⑨	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:

- 1,The Test samples should be applied to only one test item.
- 2,Sample side for each test item is 5~10pcs.
- 3,For Damp Proof Test,Pure water(Resistance > 10MΩ)should be used.
- 4,In case of malfunction defect caused by ESD damage,if it would be recovered to normal state after resetting,it would be judge as a good part.
- 5,EL evaluation should be excepted from reliability test with humidity and temperature:Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
- 6,Failure Judgment Criterion:Basic Specification Electrical Characteristic,Mechanical Characteristic,Optical Characteristic.



11. Inspection Standard

This standard apply to C-STN/TFT module

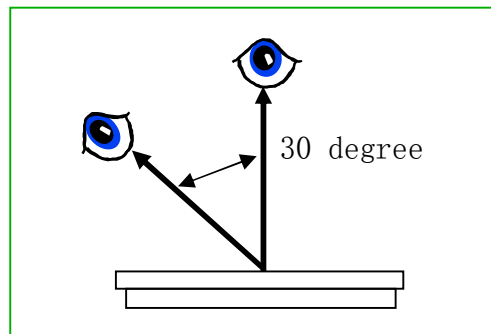
1. Spot check plan:

According to spot check level II ,MIL-STD-105D Level II ,the rank of accept or reject is below:

3A 级、2A 级: major non-conformance: AQL 0.25 minor non-conformance: AQL 0.4

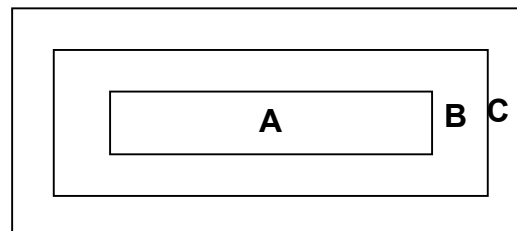
A 级: major non-conformance: AQL 0.65 minor non-conformance: AQL 1.

2. Inspection condition:



Under daylight lamp 20 ~ 40W , product distance inspector'eye 30cm,incline degree 30°.

3. LCD area define:



Area A: display area

Area B: VA area

Area C: out of VA area,not in sight after assembly

Remark :non-conformance at area C,but is OK that isn't influence raliability of product & assembly by customer.

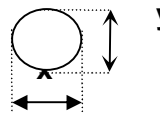


4. Inspection standard

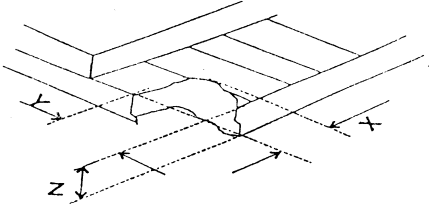
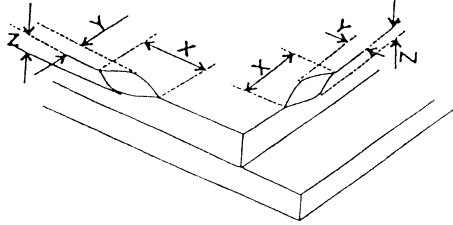
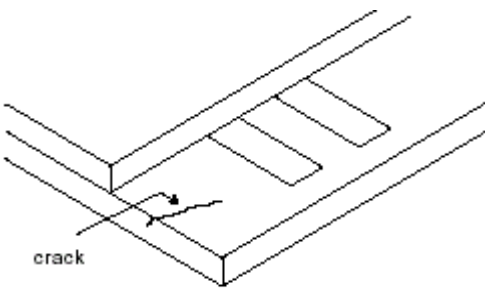
4.1 Major non-conformance

NO.	Item	Inspection standard	Rate
4.1.1	Function non-conformance	1) No display, display abnormaly 2) Miss line, short 3) B/L no function or function abnormaly 4) TP no function	major
4.1.2	miss	No matter miss what component	
4.1.3	Out of size	Module dimension out of spec	

4.2 Appearance non-conformance

NO.	Item	Inspection standard	Rate																														
4.2.1	Black or white spot (power on)	dot non-conformance define Φ $\Phi = \frac{(x+y)}{2}$ 	Minor																														
		A grade <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">area size (mm)</th> <th colspan="3">Most approve q'ty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td colspan="3">ignore</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.15$</td> <td colspan="3">3</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td colspan="3">2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td colspan="3">1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td colspan="3">0</td> </tr> </tbody> </table> Most approve 4 damages, dot to dot $\geq 10\text{mm}$		area size (mm)	Most approve q'ty			A	B	C	$\Phi \leq 0.10$	ignore			$0.10 < \Phi \leq 0.15$	3			$0.15 < \Phi \leq 0.20$	2			$0.20 < \Phi \leq 0.25$	1			$0.25 < \Phi$	0					
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4.2.2	Black or white line (power on)	A grade <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Size(mm)</th> <th colspan="3">Most approve q'ty</th> </tr> <tr> <th>L(length)</th> <th>W(width)</th> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>ignore</td> <td>$W \leq 0.03$</td> <td colspan="3">ignore</td> </tr> <tr> <td>$L \leq 5.0$</td> <td>$0.03 < W \leq 0.05$</td> <td colspan="3">2</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.05 < W \leq 0.07$</td> <td colspan="3">1</td> </tr> <tr> <td></td> <td>$0.07 < W$</td> <td colspan="3">Treat with dot non-conformance</td> </tr> </tbody> </table> Most approve 3 damages, line to line $\geq 10\text{mm}$	Size(mm)		Most approve q'ty			L(length)	W(width)	A	B	C	ignore	$W \leq 0.03$	ignore			$L \leq 5.0$	$0.03 < W \leq 0.05$	2			$L \leq 3.0$	$0.05 < W \leq 0.07$	1				$0.07 < W$	Treat with dot non-conformance			Minor
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	$0.07 < W$	Treat with dot non-conformance																															



4.2.3	Polarizer position	1) polarizer attach meet drawing, disallow out of LCD. 2) polarizer must cover display area (special require unless)	Minor												
4.2.4	LCD non-conformance	<p>(i) crash at side (remark: S=ITO length)</p>  <table border="1" data-bbox="555 548 1190 645"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0</td> <td>≤S</td> <td>ignore</td> </tr> </tbody> </table> <p>Crash disallow extend to ITO or seal.</p> <p>(ii) commonly surface scathe</p>  <table border="1" data-bbox="534 981 1211 1077"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤2.0</td> <td><frame edge</td> <td>ignore</td> </tr> </tbody> </table> <p>(iii) crack Disallow extend crack</p> 	X	Y	Z	≤3.0	≤S	ignore	X	Y	Z	≤2.0	<frame edge	ignore	Minor
X	Y	Z													
≤3.0	≤S	ignore													
X	Y	Z													
≤2.0	<frame edge	ignore													
4.2.5	Contrast voltage warp	VOP/Vlcd voltage of confirmed sample ±0.15V	Minor												
4.2.6	color	Color & luminance of module scope reference spec	Minor												
4.2.7	Cross talk	Reference confirmed limit sample	Minor												



12. Handling Precautions

12.1 Mounting method

The LCD panel of SC LCD module consists of two thin glass plates with polarizers which easily be damaged. And since the module is so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent [recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happens by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module uses C-MOS LSI drivers, so we recommend that you:

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.



12.6 storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.

[It is recommended to store them as they have been contained in the inner container at the time of delivery from us

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

13. Precaution For Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to GT LCD , and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD